Regulacijski sustavi s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora s novom pulsno-širinskom modulacijom

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SVEUČILIŠTE U SPLITU
FAKULTET ELEKTROTEHNIKE, STROJARSTVA I BRODOGRADNJE

Ivan Grgić

REGULACIJSKI SUSTAVI S IZMJENJIVAČEM KVAZI Z-TIPA NAPAJANIM IZ FOTONAPONSKOG IZVORA S NOVOM PULSNO-ŠIRINSKOM MODULACIJOM

DOKTORSKA DISERTACIJA

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REGULACIJSKI SUSTAVI S IZMJENJIVAČEM KVAZI Z-TIPA NAPAJANIM IZ FOTONAPONSKOG IZVORA S NOVOM PULSNO-ŠIRINSKOM MODULACIJOM

SAŽETAK

U ovoj doktorskoj disertaciji predstavljena su tri nova regulacijska sustava s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora. Prvi sustav je bez baterija te izmjenjivač radi u spoju s mrežom, dok su druga dva sustava s baterijama a izmjenjivač radi u jednom slučaju u spoju s mrežom, a u drugom u otočnom načinu rada. Za upravljanje izmjenjivačem kvazi Z-tipa korištena je nova pulsno-širinska modulacija, s dodanim trećim harmonikom i implementiranim mrtvim vremenom, kod koje je početak prostrijelnog stanja sinkroniziran s početkom nultog stanja i koja rezultira značajnim smanjenjem poluvodičkih gubitaka. Razvijena su dva nova algoritma za izračun poluvodičkih gubitaka izmjenjivača kvazi Z-tipa upravljanog novom pulsno-širinskom modulacijom, čija je točnost eksperimentalno provjerena.

Prvi novi regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora i spojenim na električnu mrežu osigurava praćenje točke maksimalne snage bez oscilacija i bez mjerenja struje fotonaponskog izvora. Simulacijska analiza ovog sustava provedena je za novi dinamički model fotonaponskog izvora s dvije diode i s uračunatim efektom kapaciteta osiromašenog područja i difuzijskog kapaciteta svake od dioda.

Drugi novi regulacijski sustav s baterijama potpomognutim izmjenjivačem kvazi Z-tipa u otočnom načinu rada za traženje točke maksimalne snage fotonaponskog izvora umjesto struje izvora koristi struju baterija, dok treći novi regulacijski sustav s baterijama potpomognutim izmjenjivačem kvazi Z-tipa, u mrežnom načinu rada, za istu svrhu koristi *d*-komponentu vektora struje mreže. Za sintezu oba regulacijska sustava s baterijama primijenjene su eksperimentalno potvrđene prijenosne funkcije dobivene na temelju novog lineariziranog usrednjenog matematičkog modela sustava.

KLJUČNE RIJEČI

dinamički model, fotonaponski izvor, izmjenjivač kvazi Z-tipa, mrtvo vrijeme izmjenjivača, poluvodički gubici, praćenje točke maksimalne snage, prijenosna funkcija, prostrijelno stanje, pulsno-širinska modulacija, regulacijski sustav

CONTROL SYSTEMS OF A PHOTOVOLTAIC-FED QUASI-Z-SOURCE INVERTER WITH A NOVEL PULSE-WIDTH MODULATION

ABSTRACT

This doctoral thesis presents three novel control systems of a photovoltaic-fed quasi-Z-source inverter. The first system does not contain batteries and the inverter is grid-tied, whereas the other two contain batteries and operate both in the stand-alone mode in one case and in grid-tied mode in the other. The quasi-Z-source inverter is controlled by means of a novel pulse-width modulation with injected third harmonic and implemented dead-time, where the start of a shoot-through state is synchronized with the start of a zero-switching state and which results in a significant reduction of semiconductor losses. Two novel semiconductor loss-calculation algorithms were developed for the quasi-Z-source inverter with the novel pulse-width modulation and their accuracy was experimentally evaluated.

The first proposed control system of the photovoltaic-fed, grid-tied quasi-Z-source inverter ensures the maximum power point tracking without oscillations and without measurement of the photovoltaic source current. A simulation analysis of this control system was carried with the novel dynamic two-diode model of the photovoltaic source, which accounts for diffusion and junction capacitances of both diodes.

The second proposed control system of the battery-assisted, stand-alone quasi-Z-source inverter utilizes the battery current instead of the photovoltaic source current for the maximum power point tracking of the photovoltaic source, whereas the third proposed control system of the battery-assisted, grid-tied quasi-Z-source inverter utilizes the *d*-axis grid current for the same purpose. The design of both these control systems was carried out by means of the experimentally validated transfer functions, which were obtained based on the novel small-signal model of the respective system.

KEYWORDS:

control system, dynamic model, inverter dead-time, maximum power point tracking, photovoltaic source, pulse-width modulation, quasi-Z-source inverter, semiconductor losses, shoot-through state, transfer function

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Disertacija je posvećena mojim roditeljima Franji i Stoji.

SADRŽAJ

POPIS TABLICA

POPIS SLIKA

POPIS OZNAKA I KRATICA

a	faktor idealnosti diode
B	faktor pojačanja izmjenjivača kvazi Z-tipa
cos φ	faktor snage
C_d	nadomjesni difuzijski kapacitet fotonaponskog panela
C_f	kapacitet kondenzatora u LCL filtru
C_j	nadomjesni kapacitet osiromašenog područja PN spoja fotonaponskog panela
C_{j0}	kapacitet osiromašenog područja PN spoja pri kontaktnom potencijalu φ_0
C_{ul}	kapacitet kondenzatora koji je spojen na ulaz izmjenjivača
C_1, C_2	kapacitet poprečnog i uzdužnog kondenzatora u istosmjernom krugu izmjenjivača kvazi Z-tipa, slijedom
D_{pv}	dioda u modelu fotonaponskog panela
D_{ul}	dioda na ulazu u izmjenjivač kvazi Z-tipa
D_0, d_0	srednja i trenutna vrijednost faktora trajanja prostrijelnog stanja, slijedom
$D_{0,max}$	najveća dopuštena srednja vrijednost faktora trajanja prostrijelnog stanja
D_1	dioda u istosmjernom krugu izmjenjivača kvazi Z-tipa
engl.	engleski
e_{Dcond}	trenutna vrijednost energije vođenja poredne diode
e_{D1cond}	trenutna vrijednost energije vođenja diode u istosmjernom krugu izmjenjivača
e_{Drr}	trenutna vrijednost energije oporavljanja poredne diode
e_{D1rr}	trenutna vrijednost energije oporavljanja diode u istosmjernom krugu izmjenjivača
e_{Tcond}	trenutna vrijednost energije vođenja tranzistora
e_{Toff}	trenutna vrijednost energije isklapanja tranzistora
e_{Ton}	trenutna vrijednost energije uklapanja tranzistora
f_l	frekvencija osnovnog harmonika napona i struje trošila
f_{ref}	frekvencija osnovnog harmonika modulacijskih signala
f_{sw}	frekvencija trokutastog signala nosioca
$G_{\tilde{d}_0}^{\tilde{u}_{fn}}$	prijenosna funkcija napona fotonaponskog izvora po faktoru trajanja prostrijelnog stanja
$G_{\tilde{d}_0}^{\tilde{i}_{L1}}$	prijenosna funkcija struje kroz prigušnicu L_1 po faktoru trajanja prostrijelnog stanja

$G_{\tilde{d}_0}^{\tilde{i}_{bat}}$	prijenosna funkcija struje baterija po faktoru trajanja prostrijelnog stanja
$G_{\tilde{i}_d}^{\tilde{i}_{bat}}$	prijenosna funkcija struje baterija po *d*-komponenti vektora struje mreže
i_a, i_b, i_c	trenutne vrijednosti faznih struja na izlazu filtra
$\hat{I}_a$	vršna vrijednost osnovnog harmonika struje u fazi *a* na izlazu filtra
I_{ac}	efektivna vrijednost fazne struje na izlazu filtra
i_{cd}	trenutna vrijednost struje kondenzatora s difuzijskim kapacitetom u nadomjesnoj shemi panela
i_{ce}	trenutna vrijednost struje kolektora tranzistora
i_{bat}	trenutna vrijednost struje baterija
$i_{bat\text{-}mjereno}$	izmjerena struja baterija
$i_{bat/d0\text{-}pf}$	struja baterija dobivena korištenjem prijenosne funkcije $G_{\tilde{d}_0}^{\tilde{i}_{bat}}$
$i_{bat/id\text{-}pf}$	struja baterija dobivena korištenjem prijenosne funkcije $G_{\tilde{i}_d}^{\tilde{i}_{bat}}$
i_d, i_q	trenutne vrijednosti komponenata vektora struje na izlazu filtra u sinkrono rotirajućem koordinatnom sustavu
i_d^*, i_q^*	trenutne vrijednosti komponenata referentnog vektora struje na izlazu filtra u sinkrono rotirajućem koordinatnom sustavu
i_D	trenutna vrijednost struje poredne diode tranzistora s izoliranom upravljačkom elektrodom
i_{D1}	trenutna vrijednost struje diode u istosmjernom krugu izmjenjivača kvazi Z-tipa
i_{di}	trenutna vrijednost struje diode u nadomjesnoj shemi fotonaponskog panela
i_{jd}	trenutna vrijednost struje kondenzatora s kapacitetom osiromašenog područja
i_{L1}, i_{L2}	trenutne vrijednosti struja kroz prigušnice u istosmjernom krugu izmjenjivača
I_{L1}	srednja vrijednost struje kroz prigušnicu L_1 u istosmjernom krugu izmjenjivača
i_{fn}	trenutna vrijednost struje fotonaponskog izvora
I_{ks}	srednja vrijednost struje kratkog spoja fotonaponskog panela
I_p, i_p	srednja i trenutna vrijednost struje paralelnog otpornika u nadomjesnoj shemi fotonaponskog panela, slijedom
I_{ph}, i_{ph}	srednja i trenutna vrijednost struje strujnog izvora u nadomjesnoj shemi fotonaponskog panela, slijedom
i_{pn}	trenutna vrijednost struje na ulazu u most izmjenjivača
I_{pv}, i_{pv}	srednja i trenutna vrijednost struje fotonaponskog panela, slijedom

I_0	srednja vrijednost struje zasićenja diode
k	Boltzmannova konstanta
k_D	koeficijent skaliranja zapornog napona diode
K_i	faktor promjene struje uslijed promjene temperature fotonaponskog panela
k_{ima}, k_{pma}	integracijsko i proporcionalno pojačanje regulatora napona na izlazu izmjenjivača, slijedom
k_{sw}	faktor uvećanja sklopnih energija tranzistora
k_T	koeficijent skaliranja blokirnog napona tranzistora
K_v	faktor promjene napona uslijed promjene temperature fotonaponskog panela
L_f	induktivitet prigušnica u izlaznom filtru izmjenjivača
L_1, L_2	induktiviteti prigušnica u istosmjernom krugu izmjenjivača kvazi Z-tipa
M_a	indeks amplitudne modulacije izmjenjivača
M_{a0}	početna vrijednost indeksa amplitudne modulacije izmjenjivača
MBC	signal koji definira stanje maksimalne napunjenosti baterija (od engl. maximum battery charge)
M_f	indeks frekvencijske modulacije izmjenjivača
MPP	logički signal koji definira je li postignuta točka maksimalne snage fotonaponskog izvora
N_{par}	broj paralelno spojenih fotonaponskih panela
N_{red}	ukupan broj eliminiranih sklapanja tranzistora dobiven korištenjem metode sinkronizacije s nultim stanjem umjesto konvencionalne metode
N_{ser}	broj serijski spojenih fotonaponskih panela
NS	logički signal nultog sklopnog stanja
N_{ss}	broj serijski spojenih ćelija u fotonaponskom panelu
P_{ac}	srednja vrijednost radne snage koja se predaje u mrežu
P_{dc}	srednja vrijednost ulazne snage izmjenjivača
P_{Dcond}	srednja vrijednost gubitaka vođenja porednih dioda u mostu izmjenjivača
P_{D1cond}	srednja vrijednost gubitaka vođenja diode u istosmjernom krugu izmjenjivača
P_{Drr}	srednja vrijednost gubitaka oporavljanja porednih dioda u mostu izmjenjivača
P_{D1rr}	srednja vrijednost gubitaka oporavljanja diode u istosmjernom krugu izmjenjivača
P_{fn}, p_{fn}	srednja i trenutna vrijednost snage fotonaponskog izvora, slijedom
$p_{fn\text{-}MPP\text{-}odst}$	postotno odstupanje od točke maksimalne snage

$P_{fn,max}$	maksimalna snaga fotonaponskog izvora
P_L	srednja vrijednost gubitaka prigušnica u istosmjernom krugu izmjenjivača
P_{pv}	srednja vrijednost snage fotonaponskog panela
$P_{pv,max}$	srednja vrijednost maksimalne snage koju može dati fotonaponski panel
$P_{Tcond,nST}$	srednja vrijednost gubitaka vođenja tranzistora tijekom aktivnih i nultih stanja
$P_{Tcond,ST}$	srednja vrijednost gubitaka vođenja tranzistora tijekom prostrijelnih stanja
$P_{Toff,nST}$	srednja vrijednost gubitaka isklapanja tranzistora iz aktivnih i nultih stanja
$P_{Toff,ST}$	srednja vrijednost gubitaka isklapanja tranzistora iz prostrijelnih stanja
$P_{Ton,nST}$	srednja vrijednost gubitaka uklapanja tranzistora u aktivna i nulta stanja
$P_{Ton,ST}$	srednja vrijednost gubitaka uklapanja tranzistora u prostrijelna stanja
P_{Tsw}	srednja vrijednost ukupnih sklopnih gubitaka tranzistora
R_{bat}	nadomjesni unutarnji otpor baterija
R_{ce}	dinamički otpor tranzistora
R_d	prigušni otpor u LCL filtru
R_D	dinamički otpor poredne diode
R_{D1}	dinamički otpor diode u istosmjernom krugu izmjenjivača
R_f	unutarnji radni otpor prigušnica izlaznog filtra izmjenjivača
R_{fn}	nagib pravca linearizirane strujno-naponske karakteristike fotonaponskog izvora
R_g	dodatni otpor geita tranzistora
R_{L1}, R_{L2}	unutarnji radni otpori prigušnica u istosmjernom krugu izmjenjivača
R_p	nadomjesni paralelni otpor fotonaponske ćelije
R_{pp}	nadomjesni paralelni otpor fotonaponskog panela
R_s	nadomjesni serijski otpor fotonaponske ćelije
R_{ss}	nadomjesni serijski otpor fotonaponskog panela
R_t	otpor trofaznog simetričnog trošila
s	kompleksna varijabla Laplaceove transformacije
S	upravljački signali za tranzistore u mostu izmjenjivača bez utisnutih prostrijelnih stanja
S^*	upravljački signali za tranzistore u mostu izmjenjivača s utisnutim prostrijelnim stanjima
S_n, S_p	signali prostrijelih stanja dobiveni usporedbom istosmjernih napona U_n i U_p s trokutastim signalom nosiocem

ST_{con}	signal prostrijelnog stanja dobiven prema konvencionalnoj metodi utiskivanja prostrijelnog stanja
ST_n	signal prostrijelnog stanja dobiven prema metodi sinkronizacije s nultim stanjem
ST_s	signal prostrijelnog stanja
T	trenutna temperatura fotonaponskog panela
T_c	trenutna temperatura kućišta tranzistora s ugrađenom parednom diodom
T_j	trenutna temperatura poluvodiča unutar poluvodičke sklopke
T_n	nazivna temperatura fotonaponskog panela
T_r	oznaka tranzistora u mostu izmjenjivača
T_s	period uzorkovanja signala
T_{sw}	period trokutastog signala nosioca
T_0	period prostrijelnog stanja
t_w	vremenski period u kojem se akumuliraju energije gubitaka algoritma koji radi s trenutnim vrijednostima signala
$\hat{U}_{ac}$	vršna vrijednost osnovnog harmonika napona na izlazu izmjenjivača
u_{ce}	trenutna vrijednost napona između kolektora i emitera tranzistora
$U_{ce,0}$	napon praga tranzistora
u_{C1}, u_{C2}	trenutna vrijednost napona na poprečnom i uzdužnom kondenzatoru u istosmjernom krugu izmjenjivača, slijedom
U_{C1}, U_{C2}	srednja vrijednost napona na poprečnom i uzdužnom kondenzatoru u istosmjernom krugu izmjenjivača, slijedom
u_d^*, u_q^*	trenutne vrijednosti komponenata referentnog vektora napona izmjenjivača u sinkrono rotirajućem koordinatnom sustavu
u_D	trenutna vrijednost pada napona na parednoj diodi
$U_{D,0}$	napon praga paredne diode
u_{D1}	trenutna vrijednost pada napona na diodi u istosmjernom krugu izmjenjivača
$U_{D1,0}$	napon praga diode u istosmjernom krugu izmjenjivača
U_{dc}, u_{dc}	srednja i trenutna vrijednost ulaznog napona izmjenjivača kvazi Z-tipa, slijedom
u_{fn}	trenutna vrijednost napona fotonaponskog izvora
U_{fn}^*	referentna srednja vrijednost napona fotonaponskog izvora
$U_{fn,ph}$	napon praznog hoda fotonaponskog izvora

$u_{fn/d0\text{-}pf}$	napon fotonaponskog izvora dobiven korištenjem prijenosne funkcije $G_{\tilde{d}_0}^{\tilde{u}_{fn}}$
$u_{fn/d0\text{-}pf\text{-}lit}$	napon fotonaponskog izvora dobiven korištenjem prijenosne funkcije preuzete iz literature
$u_{fn\text{-}mjereno}$	izmjereni napon fotonaponskog izvora
u_{id}, u_{iq}	trenutne vrijednosti komponenata vektora napona izmjenjivača u sinkrono rotirajućem koordinatnom sustavu
$U_{k,ref}$	referentni napon pri kojem su proizvođači snimali sklopne karakteristike tranzistora i dioda
u_{L1}, u_{L2}	trenutne vrijednosti napona na prigušnicama u istosmjernom krugu izmjenjivača
$\hat{U}_{mr}$	vršna vrijednost osnovnog harmonika mrežnog napona
u_{ma}, u_{mb}, u_{mc}	trenutne vrijednosti modulacijskih signala
u_{md}, u_{mq}	trenutne vrijednosti modulacijskih signala u sinkrono rotirajućem koordinatnom sustavu
u_{mra}, u_{mrb}, u_{mrc}	trenutne vrijednosti mrežnih napona
u_{mrd}, u_{mrq}	trenutne vrijednosti komponenata vektora napona mreže u sinkrono rotirajućem koordinatnom sustavu
U_n, U_p	istosmjerni naponi korišteni za generiranje prostrijelnih stanja kod konvencionalne metode
U_{ph}	napon praznog hoda fotonaponskog panela
U_{pv}, u_{pv}	srednja i trenutna vrijednost napona fotonaponskog panela, slijedom
U_{pn}, u_{pn}	vršna i trenutna vrijednost napona na ulazu u most izmjenjivača kvazi Z-tipa, slijedom
$\hat{U}_t$	vršna vrijednost osnovnog harmonika napona trošila
u_{tr}	trenutna vrijednost trokutastog signala nosioca
U_{0bat}	srednja vrijednost napona otvorenog kruga baterija
q	naboj elektrona
Z_n, Z	nazivna i trenutna osunčanost fotonaponskog panela, slijedom
Q_{ac}	srednja vrijednost jalove snage koja se predaje u mrežu
θ	kut vektora izlaznog napona izmjenjivača
θ_g	kut vektora mrežnog napona
τ	vrijeme života manjinskih nosioca naboja

τ_d	mrtvo vrijeme izmjenjivača kvazi Z-tipa
φ	fazni pomak između osnovnog harmonika struje i napona na izlazu izmjenjivača
φ_0	kontaktni potencijal PN spoja
ω	kružna frekvencija
ω_g	kružna frekvencija mreže

1. UVOD

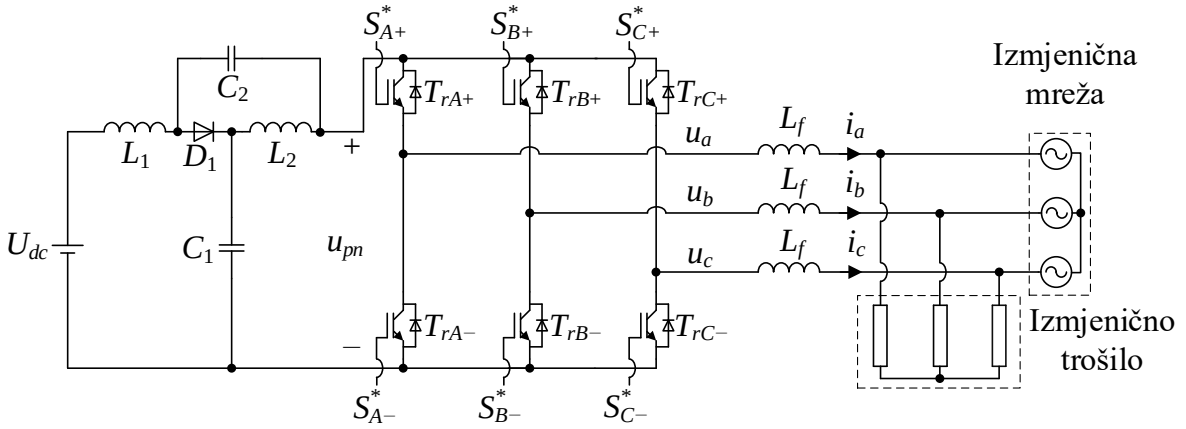
Izvorni znanstveni doprinosi ove doktorske disertacije utemeljeni su na izvornim znanstvenim doprinosima radova koji su objavljeni u znanstvenim časopisima i u zborniku radova međunarodne znanstvene konferencije. U uvodnom dijelu opisana je motivacija za izradu disertacije te su dane postavljene hipoteze. Nastavak ovog dijela donosi pregled korištenih znanstvenih metoda i izvorne znanstvene doprinose, dok je na kraju uvodnog dijela dan popis znanstvenih radova na kojima se temelje znanstveni doprinosi disertacije te pregled organizacije disertacije.

1.1. Motivacija, ciljevi i hipoteze

Svijet kakvog poznajemo danas nezamisliv je bez električne energije. Potražnja za električnom energijom raste iz godine u godinu te će se taj trend vjerojatno nastaviti i u budućnosti. Razlog tomu je sve veća cijena nafte i plina, ali i sve veća proizvodnja automobila koje pokreću električni motori. Zbog toga će u budućnosti biti jako važno osigurati proizvodnju dovoljne količine električne energije kako bi se zadovoljile rastuće potrebe tržišta. Električna energija može se proizvoditi iz neobnovljivih izvora energije i obnovljivih izvora energije. U neobnovljive izvore energije spadaju fosilna i nuklearna goriva, dok u obnovljive spadaju hidroenergija, energija vjetra, sunčeva energija, geotermalna energija, biomasa i energija mora. Glavni proizvođači električne energije koji za proizvodnju koriste neobnovljive izvore energije su termoelektrane i nuklearne elektrane. Prednost ovih elektrana je mogućnost kontrole proizvedene električne energije, a time mogućnost kontrole napona i frekvencije u električnoj mreži. Glavni nedostatci su velika proizvodnja ugljičnog dioksida kod termoelektrana te problem skladištenja nuklearnog otpada i moguće nesreće s katastrofalnim posljedicama (Černobil, Fukušima) kod nuklearnih elektrana. Osim toga, proizvodnja električne energije u ovim elektranama ovisi o dostupnosti korištenih fosilnih goriva, dok cijena proizvedene električne energije ovisi o cijeni goriva. S druge strane, proizvodnja električne energije iz obnovljivih izvora energije ekološki je prihvatljiva jer se tom prilikom ne proizvode ugljični dioksid i drugi štetni plinovi. Nadalje, obnovljivi izvori energije praktički su besplatni, međutim njihova dostupnost uglavnom je promjenjiva i ovisi o atmosferskim prilikama (npr. energija vjetra ili energija sunčevog zračenja). Fotonaponski sustavi koriste se za pretvorbu energije sunčeva zračenja u električnu energiju.

Osnovni element fotonaponskog sustava je fotonaponski izvor koji se sastoji od više međusobno spojenih fotonaponskih panela. Izvor je preko energetskih pretvarača spojen na izmjeničnu ili istosmjernu električnu mrežu ili na trošila. U Europskoj uniji se broj instaliranih fotonaponskih sustava znatno povećao u zadnjih dvadeset godina. Prema podacima iznesenim u [1], instalirana snaga fotonaponskih sustava u 2000. godini iznosila je približno 1 GW, dok je 2020. godine instalirana snaga iznosila približno 137 GW. Fotonaponski izvori se na izmjeničnu električnu mrežu spajaju preko izmjenjivača. Korištenjem tranzistora, izmjenjivači omogućavaju pretvorbu istosmjerne struje i napona fotonaponskog izvora u izmjeničnu struju i napon mreže. Zadatak regulacijskog sustava izmjenjivača je osigurati tok energije od fotonaponskog izvora prema mreži i rad fotonaponskog izvora u točki maksimalne snage. U tu svrhu moguće je koristiti izmjenjivače s utisnutim naponom [2-4] za čiji je rad, u izvedbi s jednom razinom pretvorbe potrebno da izlazni napon fotonaponskog izvora u svakom trenutku bude dovoljno velik da se na izlazu izmjenjivača može postići zadani napon mreže. To može predstavljati ograničenje u sustavima gdje temperatura panela značajnije varira jer se napon fotonaponskog izvora značajno mijenja s temperaturom. Zbog toga se u većini konvencionalnih izvedbi (s dvije razine pretvorbe) između izmjenjivača s utisnutim naponom i fotonaponskog izvora spaja istosmjerni uzlazni pretvarač [5-9], čiji je zadatak osigurati rad fotonaponskog izvora u točki maksimalne snage i osigurati dovoljan ulazni napon izmjenjivača. Implementacija uzlaznog pretvarača podrazumijeva, uz korištenje dodatnih pasivnih komponenti, korištenje dodatnog tranzistora kao i pripadajućeg upravljačkog algoritma i sklopovlja.

Izmjenjivač kvazi Z-tipa predmet je mnogih istraživanja s obzirom na to da se nametnuo kao dobra alternativa konvencionalnim rješenjima za povezivanje fotonaponskog izvora na električnu mrežu [10-23]. Topologija ovog izmjenjivača prikazana na slici 1.1 koju čine ulazni istosmjerni krug i trofazni tranzistorski most nastala je na temelju topologije izmjenjivača Z-tipa koja je predstavljena u [24]. Osnovne prednosti izmjenjivača kvazi Z-tipa u odnosu na onaj Z-tipa su kontinuirana ulazna struja izmjenjivača i niže naponsko naprezanje uzdužnog kondenzatora u istosmjernom krugu izmjenjivača.



Slika 1.1. Topologija trofaznog izmjenjivača kvazi Z-tipa [25]

Istosmjerni krug sastoji se od dvije prigušnice (L_1, L_2), dva kondenzatora (C_1, C_2) i diode (D_1). To znači da u istosmjernom krugu ovog izmjenjivača nema tranzistora što je prednost u odnosu na konvencionalna rješenja [5-9]. Tranzistorski most sastoji se od šest tranzistora T_{rA+}, T_{rA-}, T_{rB+}, T_{rB-}, T_{rC+}, T_{rC-} s porednim diodama. Tranzistori su upravljani upravljačkim signalima S^*_{A+}, S^*_{A-}, S^*_{B+}, S^*_{B-}, S^*_{C+}, S^*_{C-} s utisnutim prostrijelnim stanjima, koji su označeni na slici 1.1. Na izlazu izmjenjivača može biti spojen induktivni (L) filtar za filtriranje izlaznih struja izmjenjivača [13-15, 26-28]. Postoje također izvedbe s induktivno-kapacitivnim (LC) filtrom [10-12, 19, 29] i LCL filtrom [21, 23]. Izmjenjivač može raditi u otočnom načinu rada ako je nakon izlaznog filtra spojeno trofazno trošilo ili pak može raditi u spoju na izmjeničnu trofaznu mrežu.

Izmjenjivač kvazi Z-tipa omogućava pojačanje ulaznog napona korištenjem dodatnog sklopnog stanja- tzv. prostrijelnog stanja. Tijekom ovog sklopnog stanja, dva tranzistora iz iste grane nalaze se u stanju vođenja, zbog čega je tranzistorski most u kratkom spoju. Prostrijelno stanje moguće je implementirati u jednoj grani mosta ili istovremeno u svim granama mosta. Pojačanje ulaznog napona definira period prostrijelnog stanja (T_0), koji predstavlja ukupno trajanje svih prostrijelnih stanja koja se dogode unutar jednog perioda trokutastog signala nosioca (T_{sw}). Srednja vrijednost faktora trajanja prostrijelnog stanja definira se kako slijedi [24, 27]:

$$D_0 = \frac{T_0}{T_{sw}} \tag{1.1}$$

Vršna vrijednost osnovnog harmonika izlaznog faznog napona ($\hat{U}_{ac}$) te vršna vrijednost napona na ulazu u most izmjenjivača (U_{pn}) idealnog izmjenjivača kvazi Z-tipa definiraju se kako slijedi [27]:

$$\hat{U}_{ac} = M_a \frac{1}{1-2D_0} \frac{U_{dc}}{2} = M_a B \frac{U_{dc}}{2} \tag{1.2}$$

$$U_{pn} = \frac{1}{1-2D_0} U_{dc} = B U_{dc} \tag{1.3}$$

gdje je:

U_{dc}	srednja vrijednost napona na ulazu izmjenjivača kvazi Z-tipa
M_a	srednja vrijednost indeksa amplitudne modulacije
B	faktor pojačanja izmjenjivača kvazi Z-tipa

Srednje vrijednosti napona na poprečnom kondenzatoru C_1 (U_{C1}) i na uzdužnom kondenzatoru C_2 (U_{C2}) ovise o iznosu faktora D_0, a za idealni izmjenjivač kvazi Z-tipa računaju se kao [27]:

$$U_{C1} = \frac{1-D_0}{1-2D_0} U_{dc} \tag{1.4}$$

$$U_{C2} = \frac{D_0}{1-2D_0} U_{dc} \tag{1.5}$$

Mogućnost pojačanja ulaznog napona izmjenjivača bez korištenja dodatne upravljive poluvodičke sklopke osnovna je prednost izmjenjivača kvazi Z-tipa u odnosu na konvencionalna rješenja. Ovaj izmjenjivač moguće je koristiti u fotonaponskim sustavima za spajanje fotonaponskog izvora na izmjeničnu električnu mrežu. Nadalje, topologija izmjenjivača kvazi Z-tipa omogućava jednostavnu integraciju sustava za pohranu energije (najčešće olovno-kiselinskih baterija) u istosmjerni krug izmjenjivača, bez potrebe za dodatnim poluvodičkim pretvaračima. Zbog navedenih karakteristika, izmjenjivač kvazi Z-tipa bio je u središtu mnogih istraživanja. Hipoteze postavljene tijekom znanstvenih istraživanja provedenih prilikom izrade ove disertacije dane su kako slijedi:

1. Moguće je razviti i implementirati novu metodu utiskivanja prostrijelnih stanja zasnovanu na sinusnoj pulsno-širinskoj modulaciji s dodanim trećim harmonikom s namjerom:
   a) smanjivanja broja sklapanja tranzistora u mostu izmjenjivača kvazi Z-tipa
   b) eliminiranja neželjenog naponskog pojačanja izmjenjivača kvazi Z-tipa, koje nastaje kao posljedica neidealnih sklopnih karakteristika tranzistora.

Nova metoda bi trebala dovesti do smanjenja sklopnih gubitaka u mostu te, posljedično, povećanja korisnosti izmjenjivača. Ovu hipotezu moguće je provjeriti na temelju eksperimentalnih ispitivanja s laboratorijskom maketom izmjenjivača kvazi Z-tipa.

2. Moguće je izraditi novi algoritam za izračun poluvodičkih gubitaka izmjenjivača kvazi Z-tipa upravljanog novom pulsno-širinskom modulacijom opisanoj u 1. hipotezi. Točnost razvijenog algoritma će se provjeriti eksperimentalno.

3. Moguće je izraditi novi dinamički model fotonaponskog panela s dvije diode pri čemu se za svaku od pojedinih dioda uračunava efekt pripadajućeg kapaciteta osiromašenog područja i difuzijskog kapaciteta. Opravdanost upotrebe ovakvog modela će biti utvrđena u programskom paketu Matlab Simulink i to u slučaju samostalnog rada fotonaponskog panela kao i u sustavu regulacije izmjenjivača kvazi Z-tipa. Ovu hipotezu moguće je provjeriti u programskom paketu Matlab Simulink.

4. Moguće je izraditi novi regulacijski sustav izmjenjivača kvazi Z-tipa spojenog s električnom mrežom i napajanog iz fotonaponskog izvora pri čemu bi se praćenje točke maksimalne snage realiziralo bez oscilacija a fotonaponski izvor bi se modelirao primjenjujući model fotonaponskog panela opisan u 3. hipotezi. Ovu hipotezu moguće je provjeriti u simulacijskom modelu izrađenom u programskom paketu Matlab Simulink.

5. Moguće je izraditi novi usrednjeni matematički model sustava koji čine izmjenjivač kvazi Z-tipa napajan iz fotonaponskog izvora s baterijama spojenim paralelno uzdužnom kondenzatoru u istosmjernom krugu izmjenjivača. Na temelju ovog modela, za mala odstupanja od stacionarne radne točke, izvršit će se linearizacija te će se dobiti pripadajući linearizirani usrednjeni model. Polazeći od ovoga modela odredit će se nove prijenosne funkcije između odgovarajućih varijabli u sustavu. Valjanost usrednjenog matematičkog modela kao i novih prijenosnih funkcija moguće je provjeriti eksperimentalno na laboratorijskoj maketi izmjenjivača kvazi Z-tipa.

6. Moguće je izraditi dva nova regulacijska sustava, za otočni način rada i za spoj s mrežom, fotonaponskog sustava opisanog u 5. hipotezi. Za upravljanje izmjenjivačem kvazi Z-tipa moguće je koristiti pulsno-širinsku modulaciju opisanu u 1. hipotezi. Algoritam pomaka i promatranja korišten za praćenje točke maksimalne snage fotonaponskog izvora u predloženim regulacijskim sustavima moguće je unaprijediti

eliminacijom senzora za mjerenje struje fotonaponskog izvora koji se koristi kod klasičnog algoritma. U predloženom regulacijskom sustavu korištenom u otočnom načinu rada se umjesto struje fotonaponskog izvora može koristiti struja baterija, dok se u predloženom regulacijskom sustavu u spoju s mrežom može koristiti d-komponenta vektora struje mreže. Prijenosne funkcije dobivene u 5. hipotezi moguće je primijeniti za sintezu predloženih regulacijskih sustava te za određivanje perioda izvođenja algoritma pomaka i promatranja. Ovu hipotezu je moguće provjeriti eksperimentalno.

1.2. Znanstvene metode i znanstveni doprinosi

Sustavni pregled literature iz područja izmjenjivača kvazi Z-tipa napravljen je na početku istraživanja provedenih tijekom izrade ove disertacije. Cilj je bio proučiti postojeće metode utiskivanja prostrijelnog stanja koje se koriste kod sinusne pulsno-širinske modulacije te proučiti regulacijske sustave izmjenjivača kvazi Z-tipa napajanog iz istosmjernog izvora konstantnog napona.

U nastavku istraživanja realiziran je novi regulacijski sustav s trofaznim izmjenjivačem kvazi Z-tipa napajanim iz izvora konstantnog napona u spoju s električnom mrežom. Upravljački algoritam izmjenjivača izveden je u sinkrono rotirajućem dq koordinatnom sustavu, pri čemu je po prvi put uz pripadajuće regulatore d i q komponenti vektora struja uveden i regulator napona na izlazu izmjenjivača. Vektor izlaznog napona izmjenjivača sinkroniziran je s vektorom mrežnog napona primjenom fazno zatvorene petlje. Za upravljanje izmjenjivačem kvazi Z-tipa korištena je sinusna pulsno-širinska modulacija s dodanim trećim harmonikom, kod koje je početak prostrijelnog stanja sinkroniziran s početkom nultog sklopnog stanja. Razvijeni upravljački algoritam implementiran je u realnom vremenu korištenjem razvojnog računalnog sustava MicroLabBox (dSpace) i ispitan na laboratorijskoj maketi izmjenjivača. Rezultati ovih istraživanja dani su u znanstvenom radu [26], objavljenom na konferenciji.

Nakon realizacije regulacijskog sustava izmjenjivača kvazi Z-tipa u središtu istraživanja bili su modeli fotonaponskog panela. Sustavnim pregledom literature iz ovog područja primijećeno je da su zastupljena dva modela. Prvi model sastoji se od strujnog izvora, diode, serijskog i paralelnog otpora te se ovaj model naziva model s jednom diodom. Drugi model dobije se dodavanjem još jedne diode u model s jednom diodom i to paralelno s postojećom te se zbog toga ovaj model naziva model s dvije diode. Točnost ova dva modela provjerena je usporedbom strujno-naponskih karakteristika dobivenih korištenjem modela s odgovarajućim

izmjerenim karakteristikama za monokristalni fotonaponski panel SV60-235E (Solvis). Pokazalo se da se strujno-naponske karakteristike dobivene primjenom modela s dvije diode bolje slažu s izmjerenim te je zbog toga ovaj model unaprijeđen dodavanjem odgovarajućih kapaciteta. Po prvi put je dinamika panela modelirana dodavanjem difuzijskih kapaciteta i kapaciteta osiromašenog područja obaju dioda. Dodani kapaciteti osiromašenog područja ovise o naponu na diodama, dok dodani difuzijski kapaciteti ovise o naponu na diodama i o struji koja teče kroz diode. Simulacijski model fotonaponskog panela s dvije diode i s uračunatim promjenjivim kapacitetima izrađen je u programskom paketu Matlab Simulink pomoću osnovnih blokova. Rezultati ovih istraživanja dostupni su u znanstvenom radu objavljenom na konferenciji [I].

Novi regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora i spojenim na izmjeničnu električnu mrežu razvijen je u nastavku istraživanja. Ovaj regulacijski sustav nastao je po uzoru na sustav predložen u [26], pri čemu je na ulaz izmjenjivača spojen fotonaponski izvor. Upravljački algoritam izveden je u *dq* koordinatnom sustavu, uz korištenje fazno zatvorene petlje i regulatora napona na izlazu izmjenjivača kao i u [26]. Točka maksimalne snage fotonaponskog izvora praćena je promjenom referentne vrijednosti *d*-komponente vektora struje mreže (i_d^*), pri čemu je ulazna veličina odgovarajućeg algoritma napon fotonaponskog izvora (u_{fn}). Na ovaj način nije bilo potrebno mjeriti struju fotonaponskog izvora (i_{fn}), što je inače potrebno kod konvencionalnih algoritama (npr. algoritam pomaka i promatranja). Algoritam za praćenje točke maksimalne snage dodatno je unaprijeđen zaustavljanjem praćenja nakon postizanja točke maksimalne snage, čime se izbjegavaju oscilacije oko točke maksimalne snage. Praćenje se ponovno nastavlja ako se na temelju promjene napona fotonaponskog izvora detektira da je nastupila promjena osunčanosti ili temperature fotonaponskog izvora. Konačno, predloženi regulacijski sustav zahtijeva mjerenje samo jedne veličine u istosmjernom krugu izmjenjivača, dok postojeći sustavi u pravilu zahtijevaju mjerenje najmanje tri veličine. Ispitivanje predloženog regulacijskog sustava provedeno je simulacijski u programskom paketu Matlab Simulink. Prilikom ispitivanja korišteni su različiti modeli fotonaponskog izvora te se pokazalo da učinkovitost praćenja točke maksimalne snage ovisi o korištenom modelu fotonaponskog izvora. Rezultati istraživanja dostupni su u znanstvenom radu objavljenom u časopisu [II].

Kako bi se ispitala statička i dinamička radna svojstva otočnog sustava s izmjenjivačem kvazi Z-tipa uz regulaciju izlaznog napona izmjenjivača provedena su eksperimentalna ispitivanja. Izmjenjivač je tijekom ispitivanja bio napajan iz programibilnog istosmjernog

izvora 6200H-S (Chroma) s podešenim različitim fiksnim iznosima napona. U okviru provedenih istraživanja razmatrana je korisnost i stabilnost rada izmjenjivača za različite odnose ulaznog i izlaznog napona izmjenjivača te su određeni optimalni iznosi ulaznog napona i faktora D_0 u slučaju reguliranog izlaznog napona izmjenjivača. Rezultati ovih istraživanja objavljeni su u znanstvenom radu [30].

U nastavku istraživanja realiziran je regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora s baterijama spojenim paralelno uzdužnom kondenzatoru (C_2) u istosmjernom krugu izmjenjivača. Kod eksperimentalne izvedbe ovog sustava, programibilni istosmjerni izvor korišten je kao emulator 16 serijski spojenih fotonaponskih panela KC200GT (Kyocera). Petnaest serijski spojenih olovno-kiselinskih baterija dodano je paralelno kondenzatoru C_2 u istosmjernom krugu izmjenjivača. Upravljački algoritam korišten u otočnom načinu rada praktički je isti kao u [30], dok je u spoju s električnom mrežom korišten upravljački algoritam praktički isti kao u [26]. Struja baterija nije regulirana niti u jednom razmatranom načinu rada te je implementiran jednostavan algoritam za praćenje točke maksimalne snage fotonaponskog izvora, utemeljen na optimalno podešenom trajanju prostrijelnog stanja. Implementacija ovog algoritma ne zahtijeva mjerne senzore. Eksperimentalna provjera razmatranog sustava provedena je u širokom rasponu osunčanosti fotonaponskog izvora. Pokazalo se da statička učinkovitost praćenja točke maksimalne snage jednostavnog algoritma nije manja od 80 %. Rezultati ovih istraživanja objavljeni su u [31].

Nakon realizacije regulacijskog sustava s baterijama potpomognutim izmjenjivačem kvazi Z-tipa cilj je bio eksperimentalno odrediti gubitke izmjenjivača kvazi Z-tipa. Za potrebe ovih istraživanja bio je razmatran otočni način rada s izmjenjivačem napajanim iz programibilnog istosmjernog izvora i reguliranim izlaznim naponom izmjenjivača. U ovoj konfiguraciji baterije nisu bile spojene, a na izlaz izmjenjivača umjesto L filtra postavljen je LCL filtar kako bi se smanjilo valno izobličenje faznih struja trošila. Gubici prigušnica u istosmjernom krugu izmjenjivača izračunati su na temelju pripadajućih kataloških podataka jezgre i izmjerenog otpora namota prigušnice, dok su gubici korištenih polipropilenskih kondenzatora zanemareni zbog malog unutarnjeg otpora. Ukupni gubici računati su kao razlika mjerene ulazne i izlazne snage izmjenjivača da bi se izbjeglo računanje gubitaka LCL filtra. Rezultati istraživanja koja su provedena u [32] pokazuju da su poluvodički gubici, dobiveni kao razlika ukupnih gubitaka i gubitaka prigušnica, dominantni, čime izračun poluvodičkih gubitaka dobiva na značaju. Zbog toga su razvijena dva nova algoritma za izračun poluvodičkih gubitaka izmjenjivača kvazi Z-tipa. Oba algoritma računaju gubitke svih poluvodičkih sklopki

izmjenjivača na temelju karakteristika koje su dostupne u kataloškim podacima proizvođača. Prvi razmatrani algoritam računa gubitke uz aproksimaciju sinusne fazne struje i zanemareno valovanje struja kroz prigušnice, dok drugi algoritam računa gubitke na temelju trenutnih vrijednosti odgovarajućih mjerenih signala. Poluvodički gubici računati primjenom dvaju razmatranih algoritama uspoređeni su s izmjerenim te se pokazalo da drugi algoritam ima veću točnost. Međutim, kod oba algoritma postojala je značajna razlika između mjerenih i izračunatih poluvodičkih gubitaka, što je pripisano razlici sklopnih energija u kataloškim podacima i stvarnih sklopnih energija tranzistora. Zbog toga su sklopne energije tranzistora, u oba algoritma pomnožene s eksperimentalno određenim faktorom 1,53 te je na račun toga srednja pogreška prvog algoritma smanjena za približno 28 %, dok je srednja pogreška drugog algoritma smanjena za približno 11 %. Rezultati razmatranih istraživanja kao i detalji o dva razvijena algoritma dani su u [III].

Nova metoda utiskivanja prostrijelnih stanja u sklopna stanja sinusne pulsno-širinske modulacije razvijena je u nastavku istraživanja. Kod ove metode je, u određenom rasponu, omogućena promjena faktora D_0 neovisno o indeksu amplitudne modulacije. Prostrijelna stanja utiskuju se na početku nultih sklopnih stanja te se zbog toga ova metoda u nastavku naziva metoda sinkronizacije s nultim stanjem. Ova metoda omogućava smanjenje broja sklopnih promjena u tranzistorskom mostu unutar jednog perioda modulacijskog signala u odnosu na konvencionalnu metodu za približno četverostruki iznos indeksa frekvencijske modulacije. Kod konvencionalne metode, signal prostrijelnog stanja dobije se usporedbom dvaju istosmjernih signala (pozitivnog i negativnog) s trokutastim signalnom te se promjenom iznosa amplitude tih signala mijenja iznos faktora D_0. Zbog toga, početak prostrijelnog stanja nije sinkroniziran s početkom nultog sklopnog stanja te se između aktivnog i prostrijelnog stanja javlja dodatno nulto sklopno stanje. Implementacija metode sinkronizacije s nultim stanjem zahtijeva korištenje odgovarajućeg analognog sklopovlja postavljenog između razvojnog računalnog sustava MicroLabBox i pobudnih sklopova za tranzistore. Detaljna izvedba sklopovlja dana je u [IV]. Tijekom eksperimentalnih istraživanja provedenih kako bi se ispitala nova metoda utiskivanja prostrijelnih stanja otkriveno je postojanje dodatnog neželjenog pojačanja izmjenjivača. Ovo pojačanje posljedica je neidealnih sklopnih karakteristika tranzistora, odnosno činjenice da proces isklapanja može biti duži od procesa uklapanja tranzistora. Stoga u mostu može doći do kratkotrajnog kratkog spoja ako oba tranzistora dobiju signal za promjenu sklopnog stanja u istom trenutku. U [IV], neželjeno pojačanje eliminirano je implementacijom mrtvog vremena odgovarajućeg trajanja, kojim su

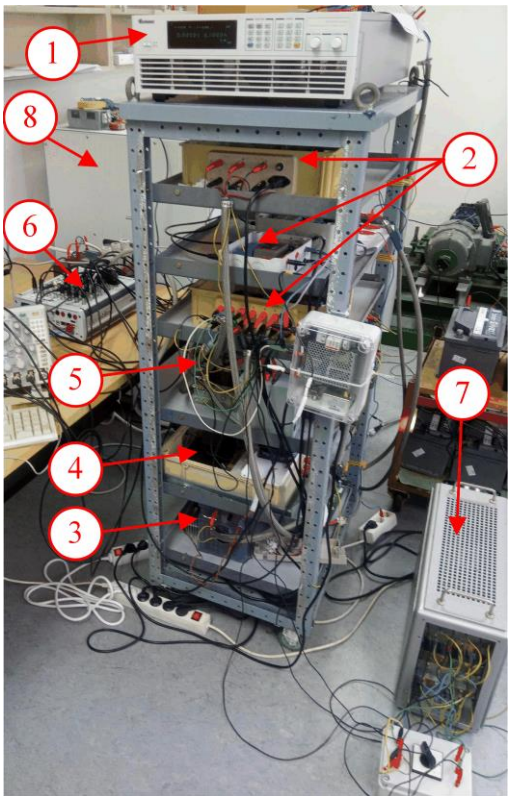
eliminirani neželjeni kratki spojevi u mostu izmjenjivača. Konačno, eksperimentalni rezultati pokazali su da se korisnost izmjenjivača poveća za 4 % kada se koristi metoda sinkronizacije s nultim stanjem u odnosnu na konvencionalnu metodu te je uočeno dodatno povećanje od 12 % u slučaju korištenja metode sinkronizacije s nultim stanjem i implementiranim mrtvim vremenom. Eksperimentalni rezultati ovih istraživanja dani su u [IV].

U nastavku istraživanja u središtu je ponovno bio regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora s baterijama spojenim paralelno uzdužnom kondenzatoru. U okviru ovih istraživanja izveden je novi usrednjeni matematički model razmatranog sustava, koji je lineariziran za mala odstupanja od stacionarne radne točke. Korištenjem linearizirаnog modela dobivene su prijenosne funkcije koje su poslužile za sintezu regulacijskog sustava u otočnom načinu rada i u spoju s mrežom te za određivanje perioda izvršavanja algoritma za praćenje točke maksimalne snage. U nastavku je unaprijeđen algoritam pomaka i promatranja koji se u razmatranom sustavu koristi za praćenje točke maksimalne snage fotonaponskog izvora. Eliminiran je mjerni senzor struje fotonaponskog izvora koji se inače koristi kod konvencionalne izvedbe ovog algoritma. Naime, struja fotonaponskog izvora zamijenjena je strujom baterija kada sustav radi u otočnom načinu rada, odnosno strujom *d*-komponente vektora struje mreže kada je sustav spojen na mrežu. Eksperimentalna ispitivanja pokazala su da algoritam pomaka i promatranja realiziran na predloženi način prati točku maksimalne snage fotonaponskog izvora jednako učinkovito kao i konvencionalni algoritam. Rad predloženog regulacijskog sustava ispitan je eksperimentalno na maketi čija je fotografija prikazana na slici 1.2, pri čemu su rezultati istraživanja objavljeni u znanstvenom radu u časopisu [V]. Dijelovi makete označeni na slici 1.2 dani su kako slijedi:

1. Programibilni istosmjerni izvor 6200H-S (Chroma) korišten je kao emulator 16 serijski spojenih fotonaponskih panela KC200GT (Kyocera).
2. Strujni senzori LA 55-P/SP52 (mjerenje faznih struja i struje baterija), naponski senzor DVL 500 (mjerenje napona fotonaponskog izvora), naponski senzori CV 3−500 (mjerenje mrežnih napona), naponski senzori LV 25–P (mjerenje napona na trošilu).
3. Istosmjerni krug izmjenjivača kvazi Z-tipa koji se sastoji od prigušnica s praškastim jezgrama T520-26 (Micrometals) ($L_1 = L_2 = 20$ mH (nezasićene)) s otporom namota $R_L = 0{,}5$ Ω (pri 25 ˚C), polipropilenskih kondenzatora MKSPI35-50U/1000 (Miflex) ($C_1 = C_2 = 50$ μF) s unutarnjim otporom od 7,8 mΩ te diode koja je sastavljena od tri

serijski spojene diodne grupe. Svaka grupa sastoji se od tri paralelno spojene poredne diode tranzistora IRG8P25N120KD (International Rectifier).

4. Trofazni tranzistorski most sačinjen od šest tranzistora s ugrađenim poredним diodama. Prvotno su korišteni tranzistori IRG8P60N120KD (International Rectifier) koji su kasnije zamijenjeni tranzistorima s većim dopuštenim naponskim naprezanjem IXBX75N170 (IXYS). U oba slučaja korišteni su isti pobudni sklopovi SKHI 22B(R) (Semikron).
5. Izlazni LCL filtar koji se sastoji od prigušnica s induktivitetima $L_{f1} = 8{,}64$ mH, $L_{f2} = 4{,}32$ mH i otporima namota $R_{f1} = 103{,}6$ mΩ, $R_{f2} = 51{,}8$ mΩ, slijedom, kondenzatora kapaciteta $C_f = 4$ μF i prigušnih otpornika $R_d = 10$ Ω.
6. Razvojni računalni sustav MicroLabBox (dSpace).
7. Simetrično trofazno radno trošilo (grijači).
8. Ormar s 25 serijski spojenih olovno-kiselinskih baterija, pri čemu su u ovom istraživanju korištene 22 serijski spojene baterije.



Slika 1.2. Fotografija laboratorijske makete izmjenjivača kvazi Z-tipa napajanog iz programibilnog istosmjernog izvora i baterija [V]

Na kraju istraživanja ponovno je razmatran izračun poluvodičkih gubitaka izmjenjivača kvazi Z-tipa. U [III], poluvodički su gubici bili računati uz korištenje metode utiskivanja prostrijelnog stanja kod koje je početak prostrijelnog stanja sinkroniziran s početkom nultog stanja. Međutim, u tom slučaju nije bilo implementirano mrtvo vrijeme u sklopna stanja sinusne pulsno-širinske modulacije jer je postojanje dodatnog neželjenog pojačanja ustanovljeno tek kasnije. Zbog toga su u novom istraživanju gubici izmjenjivača kvazi Z-tipa računati za slučaj korištenja nove metode utiskivanja prostrijelnog stanja s mrtvim vremenom. U fokusu istraživanja bio je drugi algoritam predložen u [III] koji se u tom istraživanju pokazao točnijim. Faktor korekcije sklopnih energija tranzistora ponovno je računat na isti način kao u [III] te se pokazalo da se on zbog implementacije mrtvog vremena smanji za približno 22 % (s 1,53 na 1,197). Ostali rezultati novih istraživanja gubitaka izmjenjivača kvazi Z-tipa dostupni su u znanstvenom radu danom u prilogu A koji je objavljen u časopisu International Journal of Electrical and Computer Engineering Systems.

Prethodno opisana znanstvena istraživanja provedena prilikom izrade ove disertacije rezultirala su sljedećim izvornim znanstvenim doprinosima:

1. Sinusna pulsno-širinska modulacija izmjenjivača kvazi Z-tipa s dodanim trećim harmonikom, s prostrijelnim stanjima i mrtvim vremenom koja smanjuje gubitke izmjenjivača. Za izmjenjivač kvazi Z-tipa upravljan ovom modulacijom razvijena su dva nova algoritma za izračun poluvodičkih gubitaka.
2. Regulacijski sustav s izmjenjivačem kvazi Z-tipa spojenim na električnu mrežu i napajanim iz fotonaponskog izvora koji je modeliran korištenjem novog dinamičkog modela fotonaponskog izvora. Osnovne značajke regulacijskog sustava su praćenje točke maksimalne snage bez oscilacija i bez mjerenja struje fotonaponskog izvora.
3. Regulacijski sustavi s izmjenjivačem kvazi Z-tipa s baterijama, napajanim iz fotonaponskog izvora, za mrežni i otočni način rada, utemeljeni na novom usrednjenom matematičkom modelu sustava. Algoritam pomaka i promatranja za praćenje točke maksimalne snage unaprijeđen je uklanjanjem strujnog senzora fotonaponskog izvora.

1.3. Popis objavljenih radova na kojima se temelji znanstveni doprinos rada

Ova disertacija napisana je u obliku skupa od pet objavljenih znanstvenih radova i to:

[I] I. Grgić, T. Betti, I. Marasović, D. Vukadinović i M. Bašić, Novel Dynamic Model of a Photovoltaic Module, *2018 3rd International Conference on Smart and Sustainable Technologies (SpliTech)*, 1-6, Split, Hrvatska, 2018.

[II] I. Grgić, M. Bašić i D. Vukadinović, Optimization of electricity production in a grid-tied solar power system with a three-phase quasi-Z-source inverter, Journal of Cleaner Production, 221, 656-666, 2019.

[III] I. Grgić, D. Vukadinović, M. Bašić i M. Bubalo, Calculation of Semiconductor Power Losses of a Three-Phase Quasi-Z-Source Inverter, Electronics, 9, 10, 1-19, 2020.

[IV] I. Grgić, D. Vukadinović, M. Bašić i M. Bubalo, Efficiency Boost of a Quasi-Z-Source Inverter: A Novel Shoot-Through Injection Method with Dead-Time, Energies, 14, 14, 4216, 2021.

[V] I. Grgić, D. Vukadinović, M. Bašić i M. Bubalo, Photovoltaic System with a Battery-Assisted Quasi-Z-Source Inverter: Improved Control System Design Based on a Novel Small-Signal Model, Energies, 15, 3, 850, 2022.

Radovi [II-V] objavljeni su u vodećim svjetskim časopisima referiranim u bazi *Web of Science Core Collection* ili *Current Contents Connect*. Od navedena četiri rada, radovi [II, IV, V] su objavljeni u časopisima s faktorom odjeka većim od medijana faktora odjeka časopisa iz područja elektrotehnike.

1.4. Pregled organizacije disertacije

Drugo poglavlje disertacije donosi pregled metoda utiskivanja prostrijelnog stanja za sinusnu pulsno-širinsku modulaciju te je u njemu pokazano na koji način se mogu izračunati poluvodički gubici izmjenjivača kvazi Z-tipa. U trećem poglavlju prikazani su regulacijski sustavi s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora te pregled nadomjesnih shema i karakteristika fotonaponskog izvora. Četvrto poglavlje središnjeg dijela disertacije donosi pregled regulacijskih sustava s baterijama potpomognutim izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora. Pregled znanstvenog doprinosa radova na kojima je utemeljena doktorska disertacija dan je u petom poglavlju. U šestom poglavlju disertacije dan je zaključak nakon kojeg slijedi popis relevantne literature koja je korištena prilikom izrade disertacije. Na kraju su dani prilozi, znanstveni radovi na kojima je utemeljena disertacija i životopis doktoranda.

2. UPRAVLJANJE IZMJENJIVAČEM KVAZI Z-TIPA I IZRAČUN POLUVODIČKIH GUBITAKA

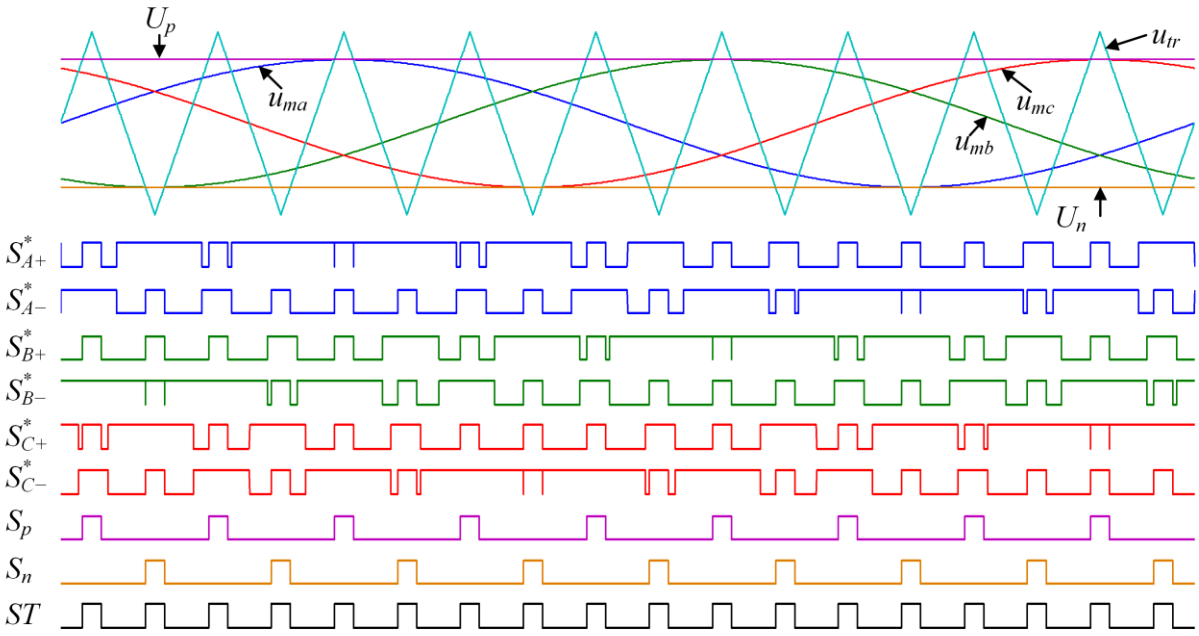
Za upravljanje tranzistorima u mostu izmjenjivača kvazi Z-tipa moguće je koristiti pulsno-širinske modulacije koje se koriste kod standardnih izmjenjivača s utisnutim naponom, npr. sinusna ili vektorska modulacija. Međutim, standardne pulsno-širinske modulacije treba dodatno prilagoditi tako da se omogući utiskivanje prostrijelnih stanja. Predloženo je više načina za utiskivanje prostrijelnih stanja za sinusnu [33-47] i vektorsku [35, 48-54] pulsno-širinsku modulaciju. Prostrijelna stanja moguće je ostvariti istovremenim uklapanjem svih tranzistora u svim granama mosta tijekom nultog sklopnog stanja ili istovremenim uklapanjem dvaju tranzistora u jednoj grani mosta koje se realizira pomicanjem referentnih signala gornjeg i donjeg tranzistora iz iste grane izmjenjivača tako da se omogući kontrolirano istovremeno vođenje oba tranzistora tj. prostrijelno stanje. Mana ovakvog načina realizacije prostrijelnih stanja u odnosu na istovremeno uklapanje svih tranzistora je veća maksimalna struja tranzistora u mostu. U nastavku je dan kratki pregled metoda za utiskivanje prostrijelnih stanja koje se koriste za sinusnu pulsno-širinsku modulaciju kod kojih su za vrijeme prostrijelnog stanja svi tranzistori u mostu uklopljeni. Naglasak je stavljen na novu metodu predloženu u [IV]. Nakon toga, analizirani su algoritmi za izračun poluvodičkih gubitaka izmjenjivača s naglaskom na nove algoritme korištene u [III].

2.1. Metode utiskivanja prostrijelnog stanja za sinusnu pulsno-širinsku modulaciju

Metode utiskivanja prostrijelnog stanja koje se koriste za sinusnu pulsno-širinsku modulaciju mogu se podijeliti u dvije skupine. U prvu skupinu spadaju metode kod kojih je srednja vrijednost faktora trajanja prostrijelnog stanja (D_0) izravno određena iznosom srednje vrijednosti indeksa amplitudne modulacije (M_a), dok u drugu skupinu spadaju metode kod kojih se iznos faktora D_0 u određenom rasponu može mijenjati neovisno o iznosu indeksa M_a. Najznačajnije metode iz prve skupine su metoda jednostavnog pojačanja, metoda maksimalnog pojačanja i metoda maksimalnog konstantnog pojačanja. Valni oblici dobiveni za metodu jednostavnog pojačanja [35, 45] (engl. *simple boost control*) prikazani su na slici 2.1. Usporedbom modulacijskih signala (u_{ma}, u_{mb}, u_{mc}) i trokutastog signala (u_{tr}) nastaju standardna sklopna stanja te se generiraju odgovarajući upravljački signali S_{A+}, S_{A-}, S_{B+}, S_{B-}, S_{C+}, S_{C-} za tranzistore T_{rA+}, T_{rA-}, T_{rB+}, T_{rB-}, T_{rC+}, T_{rC-}, slijedom. Pored standardnih sklopnih

stanja javljaju se i prostrijelna stanja. Signal prostrijelnog stanja (*ST*) rezultat je ILI logičke operacije signala S_p i S_n koji se dobiju usporedbom istosmjernih signala U_p i U_n s trokutastim signalom. Konačni upravljački signali za tranzistore s utisnutim prostrijelnim stanjima S^*_{A+}, S^*_{A-}, S^*_{B+}, S^*_{B-}, S^*_{C+}, S^*_{C-} dobiju se kao rezultat ILI logičke operacije signala *ST* i signala S_{A+}, S_{A-}, S_{B+}, S_{B-}, S_{C+}, S_{C-}. Na temelju slike 2.1 može se zaključiti da prostrijelna stanja nastupaju isključivo za vrijeme trajanja nultih sklopnih stanja, a faktor trajanja prostrijelnog stanja definira se kao:

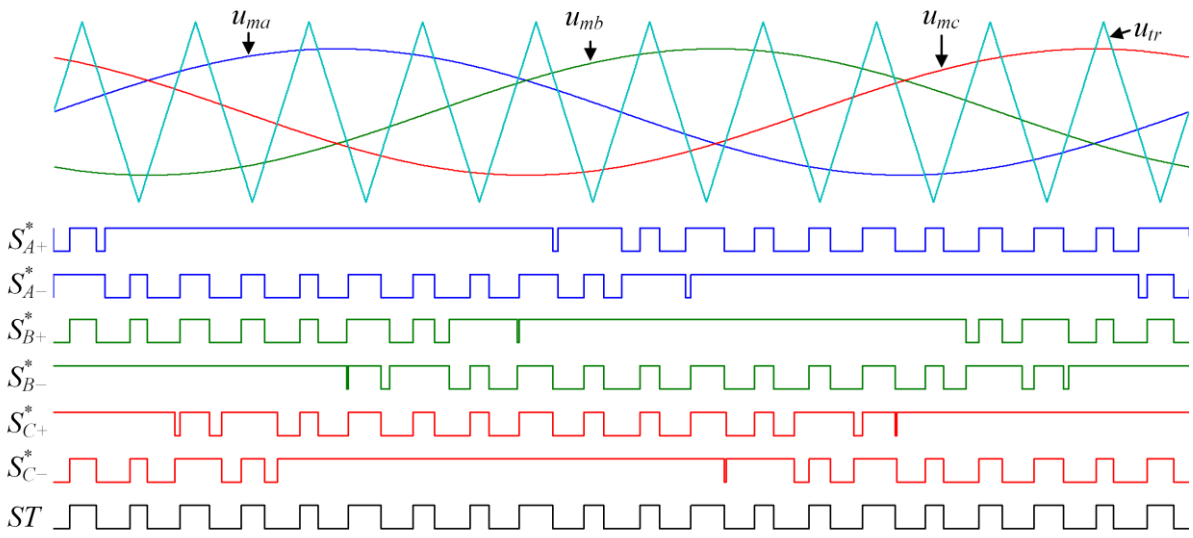
$$D_0 = \frac{T_0}{T_{sw}} = 1 - M_a \tag{2.1}$$



Slika 2.1. Valni oblici metode jednostavnog pojačanja

Kod metode maksimalnog pojačanja [45] (engl. *maximum boost control*) sva raspoloživa nulta sklopna stanja koriste se za prostrijelna stanja te se tako ostvaruje maksimalni mogući faktor pojačanja. Na temelju valnih oblika ove metode koji su prikazani na slici 2.2 može se zaključiti da je trajanje prostrijelnih stanja promjenjivo je što je posljedica promjenjivog trajanja nultih sklopnih stanja. Kao rezultat dobije se promjenjiv faktor trajanja prostrijelnog stanja s frekvencijom šest puta većom od frekvencije modulacijskih signala, a srednja vrijednost faktora D_0 računa se kako slijedi:

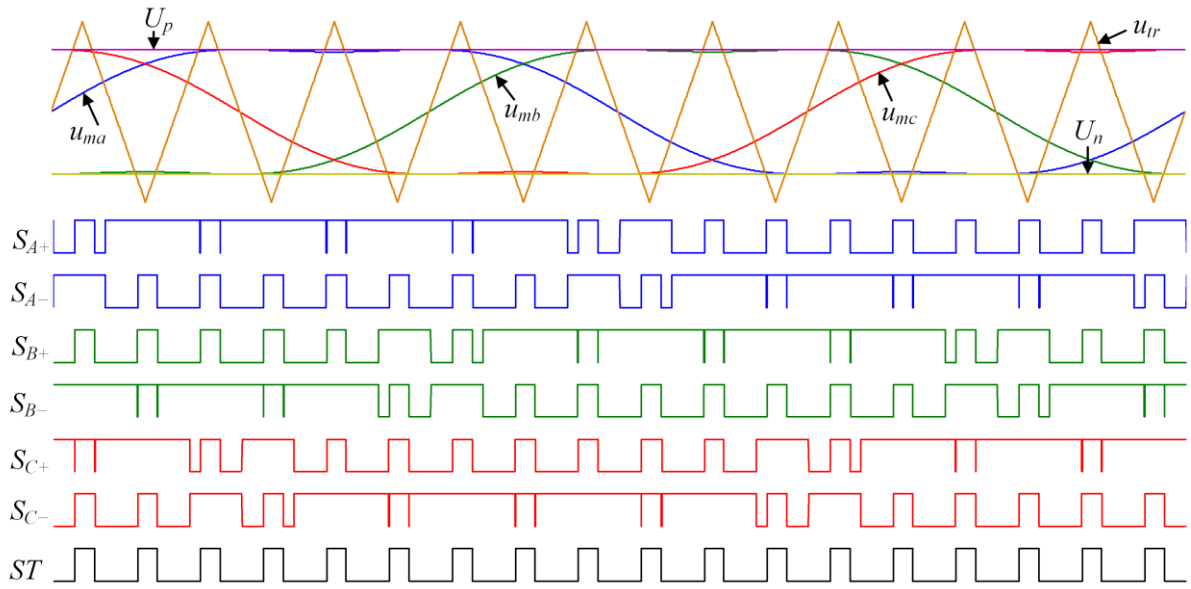
$$D_0 = \frac{T_0}{T_{sw}} = \frac{2\pi - 3\sqrt{3}M_a}{2\pi} \tag{2.2}$$



Slika 2.2. Valni oblici metode maksimalnog pojačanja

Promjenjivi iznos faktora D_0 osnovni je nedostatak metode maksimalnog pojačanja jer uzrokuje veću valovitost struja kroz prigušnice i napona na kondenzatorima u istosmjernom krugu izmjenjivača kvazi *Z*-tipa. Kako bi se postiglo maksimalno naponsko pojačanje uz konstantni iznos faktora D_0 i time što manja valovitost struja kroz prigušnice i napona na kondenzatorima koristi se metoda maksimalnog konstantnog pojačanja (engl. *maximum constant boost control*). Kod ove metode utiskivanja, prostrijelna stanja dobiju se usporedbom dvaju sinusnih signala s trokutastim signalom. Ovi sinusni signali imaju tri puta veću frekvenciju od modulacijskih signala [39]. Metoda maksimalnog konstantnog pojačanja može se dodatno unaprijediti dodavanjem trećeg harmonika u modulacijske signale [39], pri čemu njegova amplituda iznosi šestinu amplitude osnovnog harmonika [55]. Valni oblici ove metode prikazani su na slici 2.3 na kojoj se može uočiti da se i u ovom slučaju prostrijelna stanja dobivaju usporedbom dvaju istosmjernih signala (pozitivnog i negativnog) s trokutastim signalom. Maksimalni mogući iznos indeksa modulacije koji osigurava da izmjenjivač radi u linearnom načinu rada poveća se s vrijednosti 1 na $2/\sqrt{3}$. Izraz za srednju vrijednost faktora D_0 kod metode maksimalnog konstantnog pojačanja glasi:

$$D_0 = 1 - \frac{\sqrt{3}}{2} M_a \tag{2.3}$$

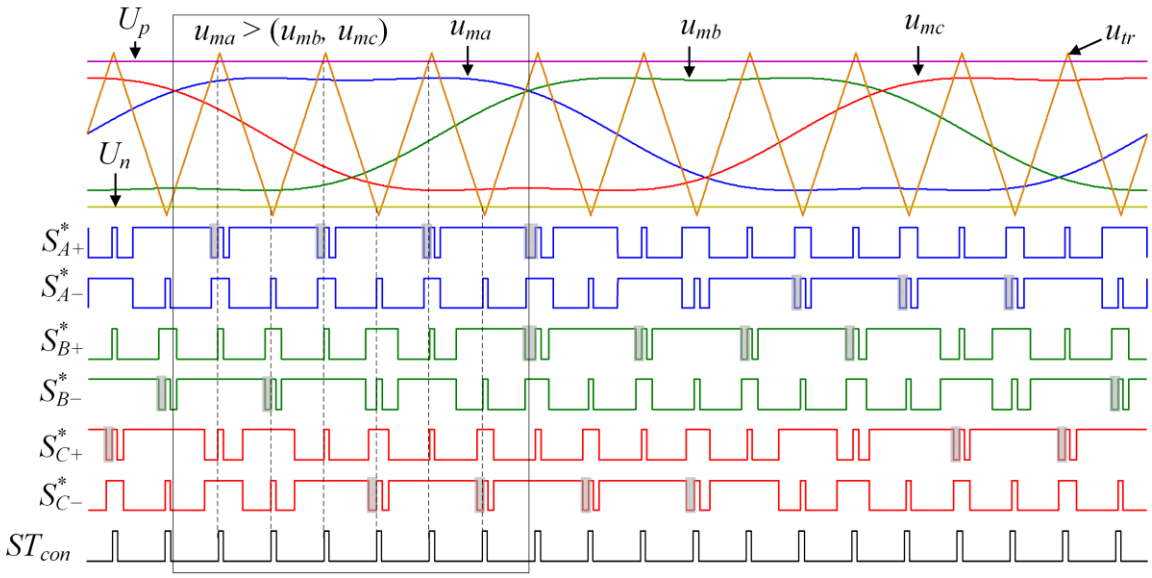


Slika 2.3. Valni oblici metode maksimalnog konstantnog pojačanja s trećim harmonikom

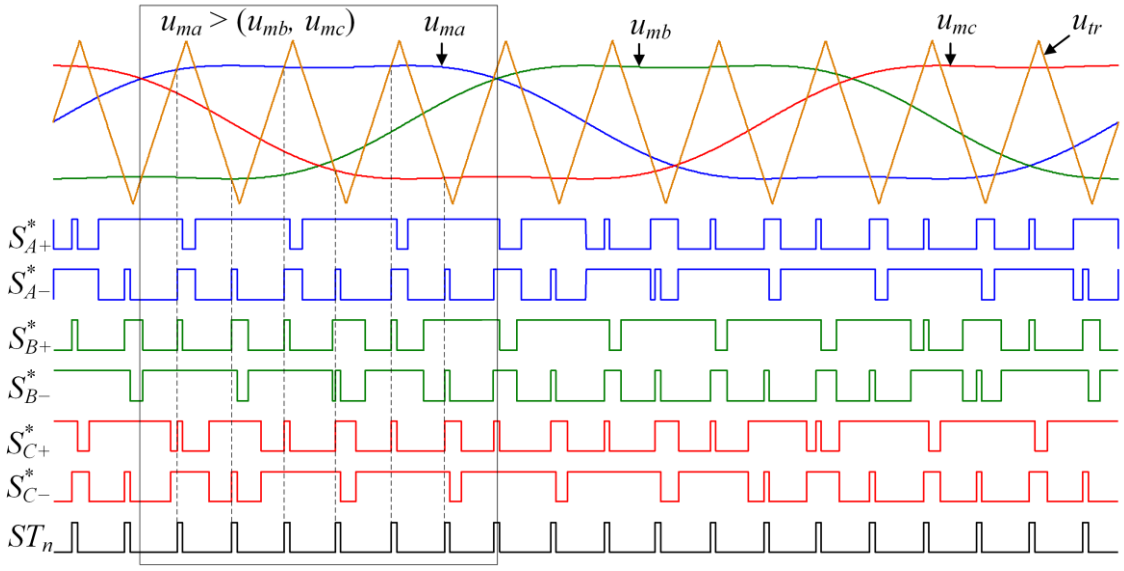
Prethodno razmatrane metode utiskivanja prostrijelnog stanja omogućavaju jedan stupanj slobode regulacijskog sustava izmjenjivača kvazi Z-tipa jer je iznos faktora D_0 uvijek određen iznosom indeksa M_a. Kako bi se omogućila dva stupnja slobode regulacijskog sustava izmjenjivača, treba osigurati promjenu iznosa faktora D_0 neovisno o iznosu faktora M_a. To se može postići korištenjem konvencionalne metode za utiskivanje prostrijelnih stanja čiji su karakteristični valni oblici, uključujući i valni oblik signala prostrijelnog stanja (ST_{con}), prikazani na slici 2.4a. Iznos faktora D_0 mijenja se promjenom iznosa istosmjernih signala U_p i U_n u rasponu od $0 \leq D_0 \leq D_{0,max}$, pri čemu se iznos $D_{0,max}$ definira za slučaj korištenja u_{ma}, u_{mb}, u_{mc} s dodanim trećim harmonikom, prema izrazu:

$$D_{0,max} = 1 - \frac{\sqrt{3}}{2} M_a \tag{2.4}$$

Slika 2.4b prikazuje valne oblike metode sinkronizacije s nultim stanjem koja je predložena u [IV], čije su osnovne značajke utiskivanje prostrijelnih stanja točno na početku nultih sklopnih stanja i upravljanje duljinom trajanja prostrijelnog stanja korištenjem integriranog kruga LM555CN. Faktor D_0 se kod ove metode može mijenjati u rasponu od $0 \leq D_0 \leq D_{0,max}$ isto kao i kod konvencionalne metode.



a)



b)

Slika 2.4. Valni oblici konvencionalne metode (a) i metode sinkronizacije s nultim stanjem (b) za utiskivanje prostrijelnih stanja koje omogućavaju istovremenu promjenu iznosa faktora D_0 i M_a [IV]

Na slici 2.4 mogu se uočiti značajne razlike u broju sklapanja tranzistora u mostu izmjenjivača između konvencionalne metode i metode sinkronizacije s nultim stanjem, iako su u oba slučaja korištene iste vrijednosti faktora D_0 i M_a. Razlike u broju sklapanja razmatrane su za upravljačke signale gornjeg tranzistora u fazi *a* (S_{A+}), a do istog zaključka bi se moglo doći razmatrajući upravljačke signale bilo kojeg drugog tranzistora u mostu izmjenjivača. Razlike u upravljačkom signalu S_{A+} između dvije razmatane metode javljaju se u intervalu kada je trenutna vrijednost modulacijskog signala faze A (u_{ma}) veća od trenutnih

vrijednosti u druge dvije faze (u_{mb}, u_{mc}). Kod metode sinkronizacije s nultim stanjem, u tom intervalu, sklopna stanja tranzistora izmjenjuju se na sljedeći način: aktivno stanje, prostrijelno stanje i nulto stanje. S druge strane, kod konvencionalne metode izmjena sklopnih stanja odvija se na sljedeći način: aktivno stanje, nulto stanje, prostrijelno stanje i nulto stanje. Na temelju ovoga može se zaključiti da kod konvencionalne metode postoje dodatna nulta sklopna stanja koja su označena sivim površinama na slici 2.4a. Posljedica postojanja tih stanja su dodatni sklopni gubici tranzistora nastali zbog isklapanja tranzistora iz aktivnog stanja u nulto stanje te ponovnog uklapanja iz nultog stanja u prostrijelno stanje.

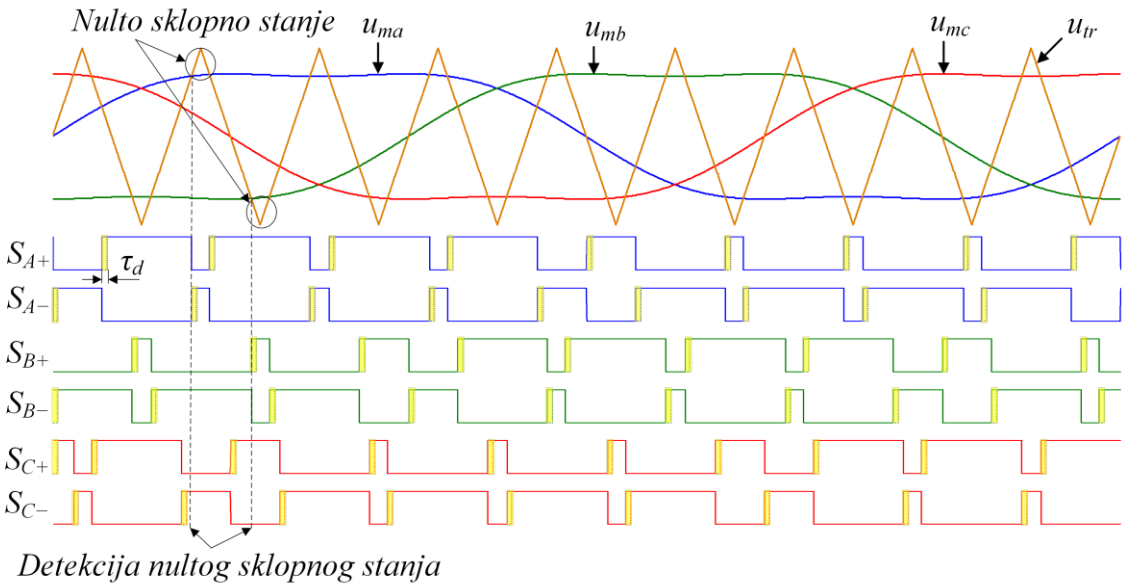
Ukupan broj dodatnih sklapanja tranzistora u konvencionalnoj metodi u odnosu na novu metodu utiskivanja ovisi o indeksu frekvencijske modulacije M_f koji se definira kao omjer frekvencije trokutastog signala nosioca (f_{sw}) i frekvencije osnovnog harmonika modulacijskih signala (f_{ref}). Na temelju slike 2.4 može se zaključiti da je kod metode sinkronizacije s nultim stanjem broj sklapanja svakog tranzistora u mostu izmjenjivača manji za dva u odnosu na konvencionalnu metodu unutar jedine trećine perioda osnovnog harmonika modulacijskog signala ($2\pi/3$). Uvažavajući navedeno, broj sklapanja tranzistora u mostu izmjenjivača unutar jednog perioda ($1/f_{ref}$) kod nove metode utiskivanja prostrijelnih stanja manji je za [IV]:

$$N_{red} \approx 6\frac{2}{3}\frac{f_{sw}}{f_{ref}} = 4M_f \tag{2.5}$$

Pokazalo se da stvarni broj smanjenih sklapanja odgovara faktoru N_{red} kada je srednja vrijednost indeksa amplitudne modulacije (M_a) jednaka ili veća od jedan ili kada je indeks M_f višekratnik broja 3. U suprotnom, stvarni broj smanjenih sklopnih stanja je neznatno veći (do pet sklopnih stanja) od izračunatog faktora N_{red}. Međutim, ovo je zanemariva pogreška jer se iznos indeksa M_f kod standardnih izmjenjivača kreće od 50 do 500 [56].

Za upravljanje izmjenjivačem kvazi Z-tipa u pravilu se koriste pulsno-širinske modulacije bez implementiranog mrtvog vremena [57, 58]. Navodi se kako mrtvo vrijeme nije potrebno implementirati zbog postojanja energetskih spremnika u istosmjernom krugu izmjenjivača te se to ističe kao prednost izmjenjivača kvazi Z-tipa. Međutim, u eksperimentalnim istraživanjima koja su provedena u [IV] otkriveno je postojanje dodatnog neželjenog pojačanja izmjenjivača. Ovo pojačanje, nastalo kao posljedica neidealnih sklopnih karakteristika tranzistora, uklonjeno je implementiranjem mrtvog vremena duljine 0,7 μs u upravljačke signale za tranzistore. Slika 2.5 prikazuje valne oblike za sinusnu pulsno-širinsku modulaciju s implementiranim mrtvim vremenom, koje je označeno žutom bojom. Mrtvo

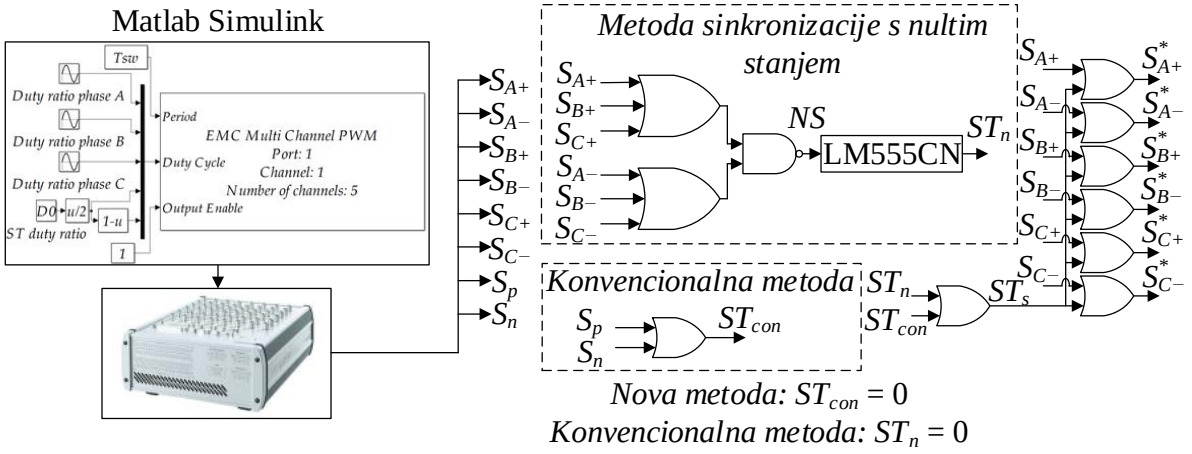
vrijeme implementira se u signale za uklapanje svih tranzistora čime se onemogućuje istovremeno vođenje dvaju tranzistora iz iste grane prilikom promjene sklopnog stanja. Početak nultog sklopnog stanja detektira se na temelju signala za isklop tranzistora jer se za isklapanje tranzistora ne implementira mrtvo vrijeme. To je prikazano na slici 2.5 za jedan sklopni period u kojem se dogode dva nulta sklopna stanja. Prvo nulto stanje nastupa u trenutku kada upravljački signal S_{A+} postane 0, dok drugo nulto sklopno stanja nastupa u trenutku kada upravljački signal S_{B-} postane 0.



Slika 2.5. Valni oblici sinusne pulsno-širinske modulacije s implementiranim mrtvim vremenom [IV]

Slika 2.6 prikazuje logički dijagram generiranja upravljačkih signala za tranzistore s utisnutim prostrijelim stanjima korištenjem metode sinkronizacije s nultim stanjem i konvencionalne metode. Upravljački signali za tranzistore generirani su na digitalnim izlazima razvojnog sustava MicroLabBox, dok je upravljački algoritam izrađen u programskom paketu Matlab Simulink. Nulta sklopna stanja detektirana su na temelju upravljačkih signala svih tranzistora. Logički signal nultog stanja (*NS*) na slici 2.6 jednak je jedinici za vrijeme nultog sklopnog stanja, dok je inače jednak nuli. Ovaj signal detektira se korištenjem dvaju ILI logičkih vrata s tri ulaza čiji su izlazi spojeni na NI logička vrata. Na prva ILI vrata spajaju se upravljački signali gornjih tranzistora dok se na druga spajaju signali donjih tranzistora. Signal *NS* bit će jednak jedinici u slučaju da je izlaz iz jednih ili obaju ILI vrata jednak nuli. Preferira se detekcija nultog stanja kada su svi logički signali gornjih tranzistora S_{A+}, S_{B+}, S_{C+} nula (prvo nulto stanje na slici 2.5) ili kada svi logički signali donjih tranzistora S_{A-}, S_{B-}, S_{C-} nula (drugo nulto stanje na slici 2.5) čime se eliminira utjecaj mrtvog

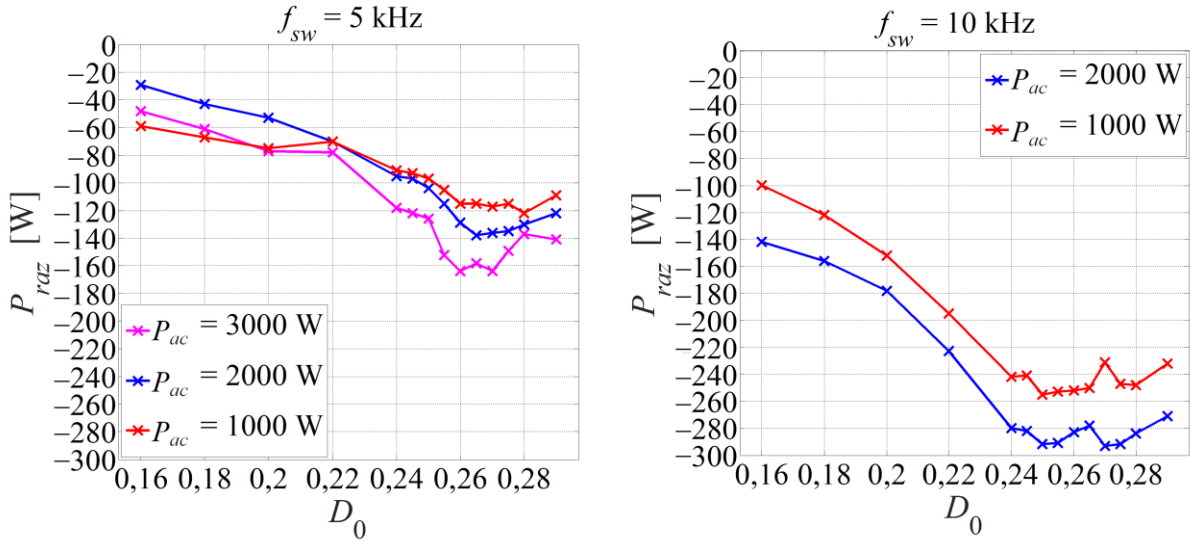
vremena na detekciju nultog stanja. Uzlazni brid signala *NS* (prijelaz iz logičke nule u jedinicu) pokreće integrirani krug LM555CN koji signal prostrijelnog stanja (ST_n) postavi u jedinicu. Trajanje pojedinačnog prostrijelnog stanja iznosi polovicu perioda prostrijelnog stanja ($T_0/2$), a ono se može podešavati promjenom upravljačkog napona dovedenog s analognog izlaza razvojnog sustava na ulaz integriranog kruga. Na kraju prostrijelnog stanja signal ST_n postaje nula i zadržava tu vrijednost do sljedećeg prostrijelnog stanja. Kod konvencionalne metode signal prostrijelnog stanja (ST_{con}) rezultat je ILI logičke operacije signala S_p i S_n koji se dobiju usporedbom signala U_p i U_n sa signalom u_{tr} (slika 2.4a). Konačni signal prostrijelnog stanja (ST_s) dobije se kao rezultat ILI logičke operacije signala ST_n i ST_{con}. Bitno je napomenuti da je prilikom korištenja konvencionalne metode signal ST_n bio postavljen u logičku nulu, dok je prilikom korištenja metode sinkronizacije s nultim stanjem signal ST_{con} bio postavljen u logičku nulu. Konačno, upravljački signali S^*_{A+}, S^*_{A-}, S^*_{B+}, S^*_{B-}, S^*_{C+}, S^*_{C-} su zapravo signali dobiveni sinusnom pulsno-širinskom modulacijom s utisnutim prostrijelnim stanjima. Detaljna izvedba sklopovlja koje je korišteno za implementaciju ove dvije metode dana je u [IV].



Slika 2.6. Generiranje upravljačkih signala za tranzistore korištenjem metode sinkronizacije s nultim stanjem i konvencionalne metode [IV]

Metoda sinkronizacije s nultim stanjem i implementiranim mrtvim vremenom uspoređena je s konvencionalnom metodom utiskivanja na temelju eksperimentalne analize gubitaka i korisnosti izmjenjivača kvazi Z-tipa [IV]. U eksperimentalnoj analizi provedenoj u [IV] uspoređeni su gubici i korisnost izmjenjivača kvazi Z-tipa dobiveni primjenom metode sinkronizacije s nultim stanjem i konvencionalne metode. U nastavku istraživanja uspoređeni su rezultati metode sinkronizacije s nultim stanjem s izostavljenim i implementiranim mrtvim vremenom te je stoga u [IV] odvojeno razmatran doprinos sinkronizacije početka prostrijelnog stanja s početkom nultog stanja i doprinos implementacije mrtvog vremena u

pogledu gubitaka i korisnosti izmjenjivača kvazi Z-tipa. Međutim, ovdje je prikazan ukupan doprinos metode sinkronizacije s nultim stanjem i implementiranim mrtvim vremenom u odnosu na konvencionalnu metodu. Slika 2.7 prikazuje razliku u gubicima izmjenjivača između konvencionalne metode i metode sinkronizacije s nultim stanjem i implementiranim mrtvim vremenom u ovisnosti o faktoru D_0 za različite vrijednosti izlazne snage (P_{ac}). Razlike su razmatrane za dva iznosa frekvencije f_{sw} = 5 kHz (Slika 2.7a) i f_{sw} = 10 kHz (Slika 2.7b), pri čemu je srednja vrijednost ulaznog napona izmjenjivača (U_{dc}) bila postavljena na 500 V, a iznos indeksa M_a bio je 0,819. Faktor D_0 mijenjao se u rasponu od 0,16 do $D_{0,max}$, koji je bio izračunat na temelju iznosa indeksa M_a prema izrazu (2.4). Bitno je naglasiti da izlaznu snagu od 3000 W nije bilo moguće ostvariti u slučaju f_{sw} = 10 kHz jer bi temperatura kućišta tranzistora s ugrađenom poredbenom diodom izmjenjivača premašila maksimalno dozvoljenu temperaturu od 130 ˚C do koje je poznata karakteristika koja opisuje sigurno područje rada tranzistora. Gubici izmjenjivača u oba slučaja računati su kao razlika srednje vrijednosti ulazne snage izmjenjivača (P_{dc}) i snage P_{ac}, dok je korisnost računata kao omjer P_{ac}/P_{dc}. Razlika gubitaka (P_{raz}) dobivena je oduzimanjem gubitaka dobivenih za konvencionalnu metodu od gubitaka dobivenih za metodu sinkronizacije s nultim stanjem i implementiranim mrtvim vremenom.

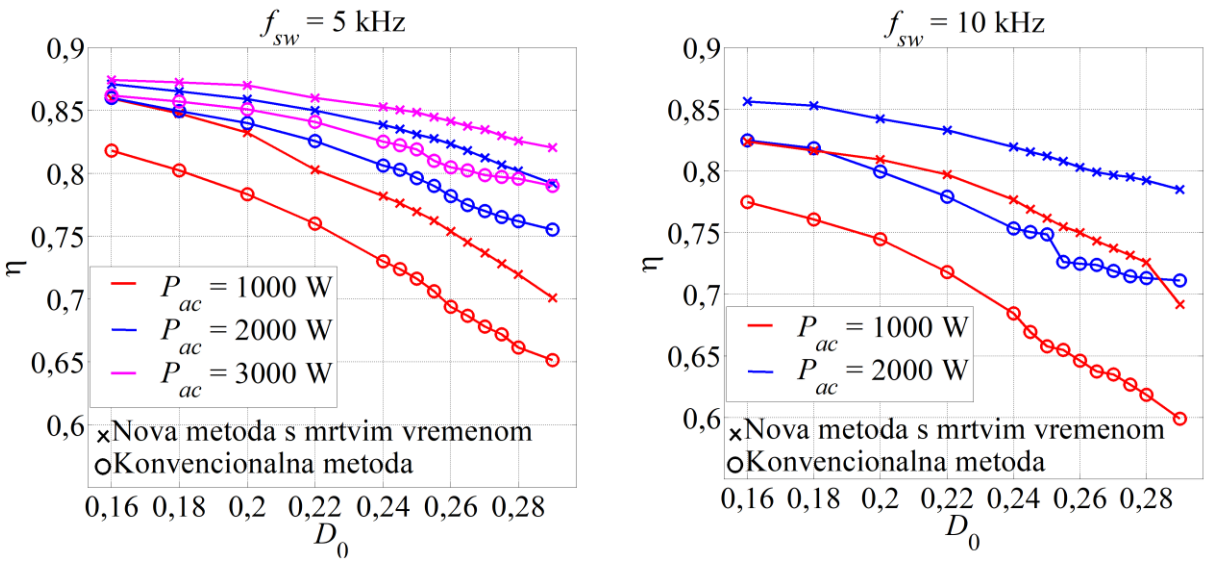


a) *b)*

Slika 2.7. Razlika u gubicima izmjenjivača kvazi Z-tipa u ovisnosti o faktoru trajanja prostrijelnog stanja pri sklopnoj frekvenciji 5 kHz (a) i 10 kHz (b)

Na slici 2.7 se može uočiti da je snaga P_{raz} za sve mjerene točke negativna što znači da su gubici u razmatranim slučajevima uvijek manji u slučaju korištenja metode sinkronizacije s nultim stanjem i implementiranim mrtvim vremenom. Apsolutni iznos snage P_{raz} raste s

porastom iznosa faktora D_0 u rasponu od 0,16 do približno 0,24, što je posljedica porasta sklopnih gubitaka zbog porasta napona U_{pn} s porastom faktora D_0. S druge strane, za iznose faktora D_0 veće od 0,24, iznos snage P_{raz} malo se mijenja za obje razmatrane sklopne frekvencije jer se s povećanjem iznosa faktora D_0 skraćuje trajanje dodatnog nultog sklopnog stanja u konvencionalnoj metodi [IV]. Zbog toga prostrijelno stanje nastupi prije nego što se tranzistor stigne prethodno u potpunosti isklopiti i realizirati nulto stanje. To dovodi do smanjenja utjecaja sinkronizacije početka nultih i prostrijelnih stanja na sklopne gubitke i posljedično do smanjenja snage P_{raz}. Dalje se može uočiti da s porastom sklopne frekvencije raste i apsolutni iznos snage P_{raz} zbog porasta broja sklapanja tranzistora te utjecaj implementacije mrtvog vremena kao i smanjenja broja sklapanja tranzistora postaje izraženiji. Smanjenje gubitaka izmjenjivača kvazi Z-tipa implementacijom nove metode utiskivanja prostrijelnog stanja s implementiranim mrtvim vremenom dovodi do povećanja korisnosti izmjenjivača. Slika 2.8 prikazuje ovisnost korisnosti izmjenjivača o faktoru D_0 za metodu sinkronizacije s nultim stanjem i implementiranim mrtvim vremenom i za konvencionalnu metodu. Korisnost izmjenjivača veća je od 2 % do 12 % ovisno o iznosu faktora D_0 kada se umjesto konvencionalne metode koristi metoda sinkronizacije s nultim stanjem i implementiranim mrtvim vremenom.

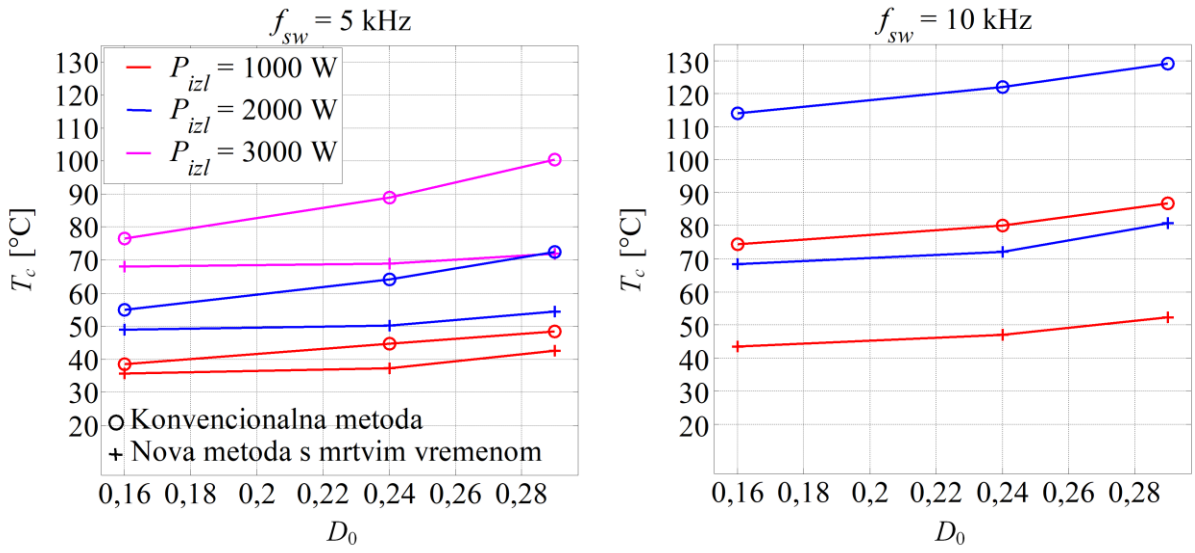


a) *b)*

Slika 2.8. Korisnost izmjenjivača kvazi Z-tipa u ovisnosti o faktoru trajanja prostrijelnog stanja za dvije razmatrane metode utiskivanja prostrijelnog stanja pri sklopnoj frekvenciji 5 kHz (a) i 10 kHz (b)

Razlike u gubicima izmjenjivača koje postoje između nove i konvencionalne metode trebale bi rezultirati različitim temperaturama kućišta tranzistora s ugrađenim porednim

diodama. Zbog toga je stacionarna temperatura kućišta jednog od tranzistora s ugrađenom poredom diodom mjerena termalnom kamerom Testo 865 (Testo). Slika 2.9 prikazuje iznos temperature kućišta (T_c) u ovisnosti o iznosu faktora D_0 za dvije razmatrane metode i dvije sklopne frekvencije 5 kHz i 10 kHz. Može se uočiti da je temperatura kućišta uvijek veća prilikom korištenja konvencionalne metode. Razlike u temperaturi kreću se od 2 ˚C pa sve do 50 ˚C. Na temelju prikazanih rezultata može se zaključiti da je korištenjem metode sinkronizacije s nultim stanjem i implementiranim mrtvim vremenom moguće povećati nazivnu snagu izmjenjivača kvazi Z-tipa za isti dozvoljeni raspon temperatura jer su gubici izmjenjivača i temperatura kućišta značajno smanjeni.



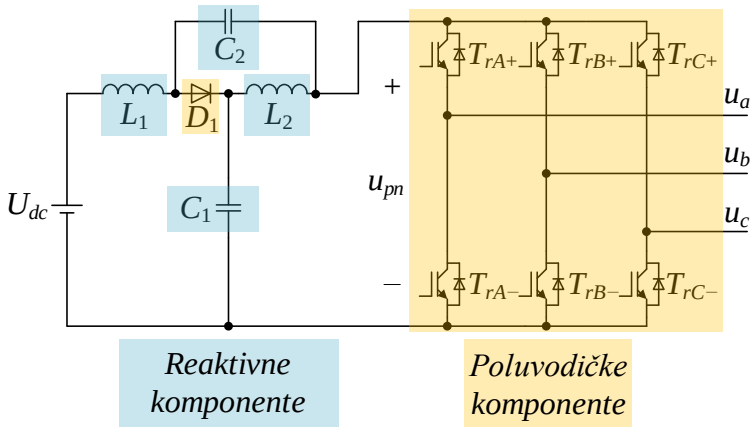
a) *b)*

Slika 2.9. Temperatura kućišta tranzistora s ugrađenom poredom diodom u ovisnosti o faktoru trajanja prostrijelnog stanja za dvije razmatrane metode utiskivanja prostrijelnog stanja pri sklopnoj frekvenciji 5 kHz (a) i 10 kHz (b) [IV]

2.2. Izračun poluvodičkih gubitaka izmjenjivača kvazi Z-tipa

Gubici izmjenjivača kvazi Z-tipa sastoje se od gubitaka reaktivnih komponenti i poluvodičkih gubitaka koji se generiraju na komponentama izmjenjivača prikazanim na slici 2.10. Ostali gubici kao npr. gubici u vodičima zanemarivi. Gubici reaktivnih komponenti obuhvaćaju gubitke dvaju prigušnica i dvaju kondenzatora u istosmjernom krugu izmjenjivača. Gubici prigušnica sastoje se od gubitaka u jezgri i Jouleovih gubitaka namota. Gubitke u jezgri, koji se sastoje od gubitaka histereze i gubitaka uslijed vrtložnih struja, moguće je izračunati korištenjem kataloških podataka proizvođača prigušnica [32]. Drugi način je primjenom tzv. modificirane Steinmetzove jednadžbe [59]. Što se tiče Jouleovih

gubitaka namota, njih je moguće odrediti na temelju mjerenog [32] ili izračunatog [59] otpora namota prigušnica. S druge strane, gubici kondenzatora u istosmjernom krugu izmjenjivača uglavnom su zanemarivi zbog malog unutarnjeg otpora kondenzatora [32].



Slika 2.10. Izmjenjivač kvazi Z-tipa s označenim komponentama koje generiraju gubitke

Poluvodičke gubitke izmjenjivača kvazi Z-tipa čine gubici tranzistora, porednih dioda i diode u istosmjernom krugu izmjenjivača. Gubici tranzistora sastoje se od gubitaka vođenja, gubitaka uklapanja, gubitaka isklapanja i gubitaka blokiranja. Na diodama se generiraju gubici vođenja, gubici uklapanja, gubici oporavljanja i reverzni gubici. Načelno se gubici blokiranja tranzistora skupa s gubicima uklapanja i reverznim gubicima diode mogu zanemariti. Postoji više načina izračuna poluvodičkih gubitaka izmjenjivača kvazi Z-tipa. U [59, 60], gubici su računati kao produkt trenutne vrijednost struje i napona tranzistora i dioda izmjenjivača. Ovaj način izračuna gubitaka ne zahtijeva poznavanje strujno-naponskih karakteristika poluvodiča kao ni sklopnih energija poluvodiča. Međutim, mjerni članovi koji se u ovom slučaju koriste za mjerenje struje i napona poluvodiča moraju imati širok frekvencijski opseg kako bi točno izmjerili brzo promjenjive struje i napone. Dalje, u ovom slučaju, ne smije postojati vremenski pomak između mjerene struje i napona jer on dovodi do pogrešnog izračuna gubitaka. Drugi način izračuna poluvodičkih gubitaka je korištenjem kataloških podataka poluvodiča [49, 61, 62], [III]. Za izračun gubitaka vođenja koriste se strujno-naponske karakteristike poluvodiča, dok se za izračun sklopnih gubitaka koriste sklopne energije poluvodiča. Strujno-naponske karakteristike poluvodiča obično se aproksimiraju dvama pravcima pomoću kojih se odredi napon praga i dinamički otpor poluvodiča.

U istraživanjima provedenim u [III] most izmjenjivača kvazi Z-tipa bio je sastavljen od tranzistora s ugrađenim porednim diodama IRG8P60N120KD (International Rectifier), dok je dioda u istosmjernom krugu bila sastavljena od četiri paralelno spojene poredne diode

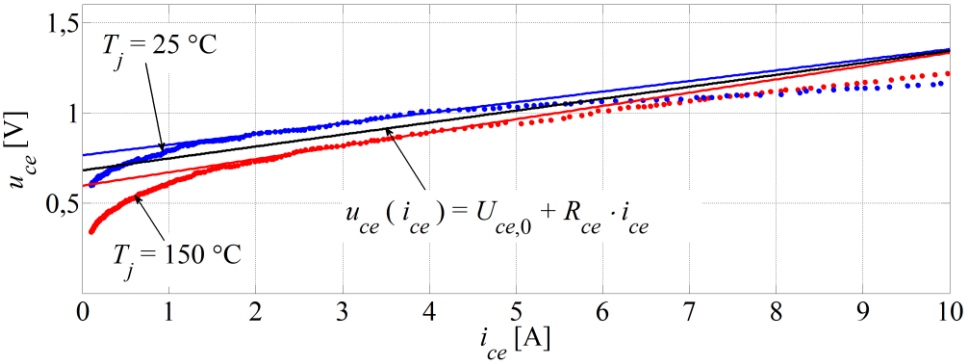
tranzistora IRG8P25N120KD (International Rectifier). Na slici 2.11 prikazana je aproksimacija strujno-naponskih karakteristika tranzistora s ugrađenom poprednom diodom IRG8P60N120KD. Napon praga tranzistora ($U_{ce,0}$) i dinamički otpor (R_{ce}) određeni su za dvije dane temperature poluvodiča T_j = 25 ˚C i T_j = 150 ˚C aproksimacijom odgovarajućih karakteristika za struje kolektora manje od 10 A jer struja kolektora u eksperimentima nije prelazila 8 A. Konačni iznosi faktora $U_{ce,0}$ i R_{ce}, dani u prilogu B, određeni su usrednjavanjem vrijednosti dobivenih za dvije temperature te je konačno strujno-naponska karakteristika tranzistora aproksimirana kao:

$$u_{ce} = U_{ce,0} + i_{ce} R_{ce} \tag{2.6}$$

gdje je:

u_{ce} trenutna vrijednost napona između kolektora i emitera tranzistora

i_{ce} trenutna vrijednost struje kolektora tranzistora



Slika 2.11. Aproksimacija strujno-naponskih karakteristika tranzistora s poprednom diodom IRG8P60N120KD

Strujno-naponske karakteristike poredne diode tranzistora i diode u istosmjernom krugu izmjenjivača aproksimirane su na isti način kao i karakteristike tranzistora te se dobije:

$$\begin{aligned} u_D &= U_{D,0} + i_D R_D \\ u_{D1} &= U_{D1,0} + i_{D1} R_{D1} \end{aligned} \tag{2.7}$$

gdje je:

u_D trenutna vrijednost pada napona na poprednoj diodi

i_D trenutna vrijednost struje poredne diode

u_{D1} trenutna vrijednost pada napona na diodi u istosmjernom krugu

i_{D1} trenutna vrijednost struje diode u istosmjernom krugu

$U_{D,0}$ napon praga poredne diode (iznos dan u prilogu B)

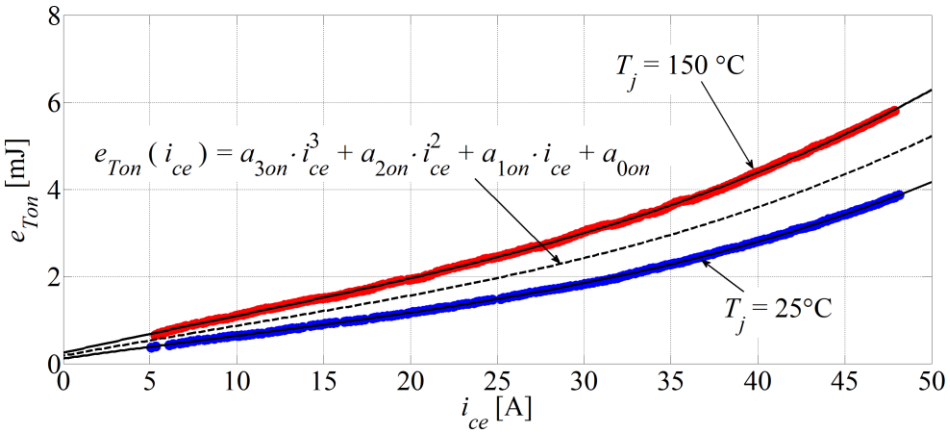
R_D dinamički otpor poredne diode (iznos dan u prilogu B)

$U_{D1,0}$ napon praga diode u istosmjernom krugu izmjenjivača (iznos dan u prilogu B)

R_{D1} dinamički otpor diode u istosmjernom krugu izmjenjivača (iznos dan u prilogu B)

Sklopne energije dobiju se iz kataloških podataka poluvodiča aproksimacijom odgovarajućih karakteristika sklapanja. Kao primjer na slici 2.12. prikazana je aproksimacija karakteristika koje opisuju energije uklapanja (e_{Ton}) u ovisnosti o struji kolektora (i_{ce}) tranzistora IRG8P60N120KD. Ove karakteristike, dane za dvije temperature poluvodiča T_j = 25 ˚C i T_j = 150 ˚C, aproksimirane su polinomima trećeg stupnja u širem rasponu struje i_{ce} u odnosu na karakteristike prikazane na slici 2.11. To je napravljeno kako bi se što točnije aproksimirale karakteristike za struje i_{ce} manje od 5 A jer u tom području proizvođač nije definirao karakteristike. Konačni izraz za energiju uklapanja tranzistora dobiven je usrednjavanjem koeficijenata dobivenih aproksimacijom karakteristika za dvije razmatrane temperature te je dan kako slijedi:

$$e_{Ton}(i_{ce}) = k_{sw}\left(\frac{U_{pn}}{U_{k,ref}}\right)^{k_T}\left(a_{3on}i_{ce}^3 + a_{2on}i_{ce}^2 + a_{1on}i_{ce} + a_{0on}\right) \tag{2.8}$$



Slika 2.12. Aproksimacija energije uklapanja tranzistora s poredbenom diodom IRG8P60N120KD

Iznosi koeficijenata a_{3on}, a_{2on}, a_{1on} i a_{0on}, koji se koriste u izrazu (2.8), dani su u prilogu B. Iznos sklopnih energija uvelike ovisi o iznosu otpora R_g koji se nalazi u krugu geita tranzistora te o iznosu blokirnog napona tranzistora. Vrijednost otpora R_g obično se postavi na vrijednost koja odgovara onoj za koju su snimane karakteristike dane u kataloškim podacima tranzistora (u ovom slučaju R_g = 10 Ω). S druge strane, iznos blokirnog napona tranzistora, jednak iznosu napona U_{pn}, promjenjiv je te zbog toga u izrazu (2.8) postoji faktor skaliranja

$\left(U_{pn}/U_{k,ref}\right)^{k_T}$, gdje je $U_{k,ref}$ referentni napon pri kojem su snimane karakteristike (u ovom slučaju $U_{k,ref}$ = 600 V). Faktor k_T u eksperimentu predstavlja koeficijent skaliranja blokirnog napona tranzistora i kreće se u rasponu od 1 do 1,4 [63, 64]. Faktor k_{sw} koji se također pojavljuje u izrazu (2.8) predstavlja faktor uvećanja sklopnih energija tranzistora [III]. Obično se inicijalno postavlja k_{sw} = 1, ali ovaj faktor može poprimiti i veće vrijednosti. Ovaj faktor uveden je pod pretpostavkom da su sklopne energije tranzistora u laboratorijskoj izvedbi izmjenjivača kvazi Z-tipa veće od energija koje su dane u kataloškim podacima, koje su snimane primjenom testa dvostrukog impulsa. Razlike u energijama su posljedica postojanja dodatnih parazitnih kapaciteta i induktiviteta tranzistora u laboratorijskoj izvedbi izmjenjivača u odnosu na test dvostrukog impulsa [65]. Energije isklapanja tranzistora također su aproksimirane polinomima trećeg stupnja s koeficijentima a_{3off}, a_{2off}, a_{1off} i a_{0off}, čiji su iznosi dani u prilogu B. Konačno, za energiju isklapanja koriste se faktori skaliranja i uvećanja te se ona definira kao:

$$e_{Toff}\left(i_{ce}\right) = k_{sw}\left(\frac{U_{pn}}{U_{k,ref}}\right)^{k_T}\left(a_{3off}i_{ce}^3 + a_{2off}i_{ce}^2 + a_{1off}i_{ce} + a_{0off}\right) \tag{2.9}$$

Karakteristike koje opisuju energije oporavljanja poredne diode (e_{Drr}) i diode u istosmjernom krugu (e_{D1rr}) u ovisnosti o strujama dioda i_D i i_{D1}, slijedom, aproksimirane su polinomima trećeg stupnja. Iznosi pripadajućih koeficijenata a_{3D}, a_{2D}, a_{1D}, a_{0D}, a_{3D1}, a_{2D1}, a_{1D1} i a_{0D1} dani su u prilogu B. Ove energije skaliraju se primjenom faktora $\left(U_{pn}/U_{k,ref}\right)^{k_D}$, gdje je k_D koeficijent skaliranja zapornog napona diode čiji se iznos kreće u rasponu od 0,5 do 0,6 [64], te su dane kako slijedi:

$$\begin{aligned} e_{Drr}\left(i_D\right) &= \left(\frac{U_{pn}}{U_{k,ref}}\right)^{k_D}\left(a_{3D}i_D^3 + a_{2D}i_D^2 + a_{1D}i_D + a_{0D}\right) \\ e_{D1rr}\left(i_{D1}\right) &= \left(\frac{U_{pn}}{U_{k,ref}}\right)^{k_D}\left(a_{3D1}i_{D1}^3 + a_{2D1}i_{D1}^2 + a_{1D1}i_{D1} + a_{0D1}\right) \end{aligned} \tag{2.10}$$

Poluvodički gubici izmjenjivača kvazi Z-tipa u [61, 62] računati su uz korištenje linearne aproksimacije sklopnih energija tranzistora i dioda s obzirom na struju. Međutim, točnija aproksimacija dobije se primjenom polinoma trećeg stupnja što je napravljeno u [III]. Nadalje, u [III] su predložena dva nova algoritma za izračun poluvodičkih gubitaka izmjenjivača kvazi Z-tipa, koja su ukratko opisana u nastavku. Oba algoritma računaju

gubitke tranzistora i poprednih dioda u mostu izmjenjivača te gubitke diode u istosmjernom krugu. Što se tiče gubitaka u mostu, računaju se gubici jednog tranzistora i njegove poredne diode te se oni, uz pretpostavku simetrije, množe sa šest kako bi se odredili ukupni gubici u mostu izmjenjivača.

Prvi algoritam za izračun poluvodičkih gubitaka izmjenjivača kvazi Z-tipa, označen u [III] kao LCA1 (od engl. *loss-calculation algorithm*), utemeljen je na algoritmima koji su korišteni za konvencionalne izmjenjivače s naponskim ulazom [66-68]. Ovaj algoritam pogodan je za izračun gubitaka izmjenjivača upravljanog novom pulsno-širinskom modulacijom, koja je opisana u prethodnom potpoglavlju. Pri izračunu gubitaka vrijede sljedeće pretpostavke: sinusna fazna struja, zanemarivo valovanje struje kroz prigušnicu i zanemariv utjecaj mrtvog vremena. Gubici vođenja tranzistora računati su odvojeno za aktivna i nulta stanja ($P_{Tcond,nST}$) te za prostrijelna stanja ($P_{Tcond,ST}$), a dani su kako slijedi [III]:

$$P_{Tcond,nST} = U_{ce,0}\hat{I}_a\left(\frac{1-D_0}{2\pi}+\frac{M_a\cos(\varphi)}{8}\right)+R_{ce}\hat{I}_a^2\left(\frac{1-D_0}{8}+\frac{M_a\cos(\varphi)}{3\pi}-\frac{M_a\cos(3\varphi)}{90\pi}\right)$$
$$P_{Tcond,ST} = D_0\left[R_{ce}\left(\frac{4}{9}I_{L1}^2+\frac{1}{8}\hat{I}_a^2\right)+U_{ce,0}\frac{2}{3}I_{L1}\right] \quad (2.11)$$

gdje je:

$\hat{I}_a$ vršna vrijednost osnovnog harmonika struje u fazi *a* na izlazu izmjenjivača

φ fazni pomak između osnovnog harmonika struje i napona na izlazu izmjenjivača

I_{L1} srednja vrijednost struje kroz prigušnicu L_1 u istosmjernom krugu izmjenjivača

Ukupni gubici vođenja svih tranzistora u mostu izmjenjivača dobiju se tako da se gubici $P_{Tcond,nST}$ i $P_{Tcond,ST}$ izračunati prema izrazima (2.11) zbroje i pomnože sa šest. Gubici vođenja svih poprednih dioda u mostu izmjenjivača izračunati su na temelju odgovarajućih energija vođenja, prema izrazu:

$$P_{Dcond} = 6\left[U_{D,0}\hat{I}_a\left(\frac{1-D_0}{2\pi}-\frac{M_a\cos(\varphi)}{8}\right)+R_D\hat{I}_a^2\left(\frac{1-D_0}{8}-\frac{M_a\cos(\varphi)}{3\pi}+\frac{M_a\cos(3\varphi)}{90\pi}\right)\right] \quad (2.12)$$

Gubici vođenja diode u istosmjernom krugu izmjenjivača računati su uz pretpostavku konstantne srednje vrijednosti struje kroz prigušnicu, kako slijedi [III]:

$$P_{D1cond} = (1-D_0)\left(R_{D1}I_{L1}^2+U_{D1,0}I_{L1}\right) \quad (2.13)$$

Sklopni gubici tranzistora sastoje se od sklopnih gubitaka nastalih zbog sklapanja između aktivnih i nultih stanja izmjenjivača te onih nastalih zbog sklapanja između aktivnih ili nultih stanja i prostrijelnih stanja. Gubici uklapanja ($P_{Ton,nST}$) i isklapanja tranzistora ($P_{Toff,nST}$) uzrokovani sklapanjima između aktivnih i nultih stanja računaju se kao:

$$\begin{aligned} P_{Ton,nST} &= \frac{e_{Ton}\left(\hat{I}_a\right)}{\pi} f_{sw} \cos(\varphi) \\ P_{Toff,nST} &= \frac{e_{Toff}\left(\hat{I}_a\right)}{\pi} f_{sw} \cos(\varphi) \end{aligned} \tag{2.14}$$

Izračun sklopnih gubitaka nastalih uslijed sklapanja između aktivnih ili nultih sklopnih stanja i prostrijelnih stanja je složeniji. On ovisi o broju uklapanja u prostrijelno stanje i broju isklapanja iz prostrijelnog stanja unutar jednog sklopnog perioda (T_{sw}). Međutim, pokazalo se da se ovi brojevi mijenjaju unutar jednog perioda osnovnog harmonika sinusnog signala ($1/f_{ref}$), što je posljedica korištenja nove metode za utiskivanje prostrijelnih stanja. U [III] su izvedena dva izraza za izračun gubitaka nastalih uklapanjem tranzistora u prostrijelno stanje ($P_{Ton,ST}$), odnosno dva izraza za izračun gubitaka nastalih isklapanjem tranzistora iz prostrijelnog stanja ($P_{Toff,ST}$). Koji će se izraz koristiti ovisi o iznosu kuta φ, a kada vrijedi $0 \leq \varphi \leq \pi/6$, gubici se računaju kako slijedi [III]:

$$\begin{aligned} P_{Ton,ST} &= f_{sw}\left[\frac{7}{6} e_{Ton}\left(\frac{2}{3} I_{L1}\right) - \frac{\sqrt{3}\cos(\varphi)+2}{2\pi} e_{Ton}\left(\frac{\hat{I}_a}{2}\right)\right] \\ P_{Toff,ST} &= f_{sw}\left[\frac{3}{2} e_{Toff}\left(\frac{2}{3} I_{L1}\right) - \frac{1}{\pi} e_{Toff}\left(\frac{\hat{I}_a}{2}\right) - \frac{\sqrt{3}\cos(\varphi)}{2\pi} e_{Toff}\left(\hat{I}_a\right)\right] \end{aligned} \tag{2.15}$$

Odnosno, kada vrijedi $\pi/6 \leq \varphi \leq \pi/2$, ovi gubici se računaju kao:

$$\begin{aligned} P_{Ton,ST} &= f_{sw}\left[\left(1+\frac{\varphi}{\pi}\right) e_{Ton}\left(\frac{2}{3} I_{L1}\right) - \frac{\sqrt{3}\cos(\varphi)+2}{2\pi} e_{Ton}\left(\frac{\hat{I}_a}{2}\right) - e_{Ton}\left(\hat{I}_a\right)\frac{1-\cos(\varphi-\pi/6)}{2\pi}\right] \\ P_{Toff,ST} &= f_{sw}\left[\frac{3}{2} e_{Toff}\left(\frac{2}{3} I_{L1}\right) - \frac{1}{\pi} e_{Toff}\left(\frac{\hat{I}_a}{2}\right) - \frac{\cos(\varphi+\pi/6)+1}{2\pi} e_{Toff}\left(\hat{I}_a\right)\right] \end{aligned} \tag{2.16}$$

Ukupni sklopni gubici tranzistora u mostu izmjenjivača računaju se kako slijedi:

$$P_{Tsw} = 6\left(P_{Ton,nST} + P_{Toff,nST} + P_{Ton,ST} + P_{Toff,ST}\right) \tag{2.17}$$

Poredna dioda gornjeg tranzistora u mostu izmjenjivača oporavlja se svaki put kada se donji tranzistor u istoj grani mosta uklapa. Prema tome, broj oporavljanja poredne diode

unutar jednog sklopnog perioda (T_{sw}) je vezan za broj uklapanja tranzistora. Zbog toga su ukupni gubici oporavljanja svih poredni dioda u mostu (P_{Drr}) također određeni s obzirom na iznos kuta φ, a kada vrijedi $0 \leq \varphi \leq \pi/6$, ovi gubici računaju se kao:

$$P_{Drr} = 6 f_{sw} \frac{4 - \sqrt{3}\cos(\varphi)}{2\pi} e_{Drr}\left(\hat{I}_a\right) \tag{2.18}$$

Odnosno, kada vrijedi $\pi/6 \leq \varphi \leq \pi/2$, ovi gubici računaju se kao:

$$P_{Drr} = 6 f_{sw} \frac{\sin(\varphi) - \sqrt{3}\cos(\varphi) + 6}{4\pi} e_{Drr}\left(\hat{I}_a\right) \tag{2.19}$$

Dioda u istosmjernom krugu izmjenjivača oporavlja se svaki put kada nastupi prostrijelno stanje, tj. dva puta unutar jednog sklopnog perioda. Uzme li se to u obzir gubici oporavljanja diode u istosmjernom krugu izmjenjivača (P_{D1rr}) računaju se kao:

$$P_{D1rr} = 2 f_{sw} e_{D1rr}\left(I_{L1}\right) \tag{2.20}$$

Detaljni izvodi jednadžbi (2.11)-(2.20), koje čine prvi algoritam, dani su u [III].

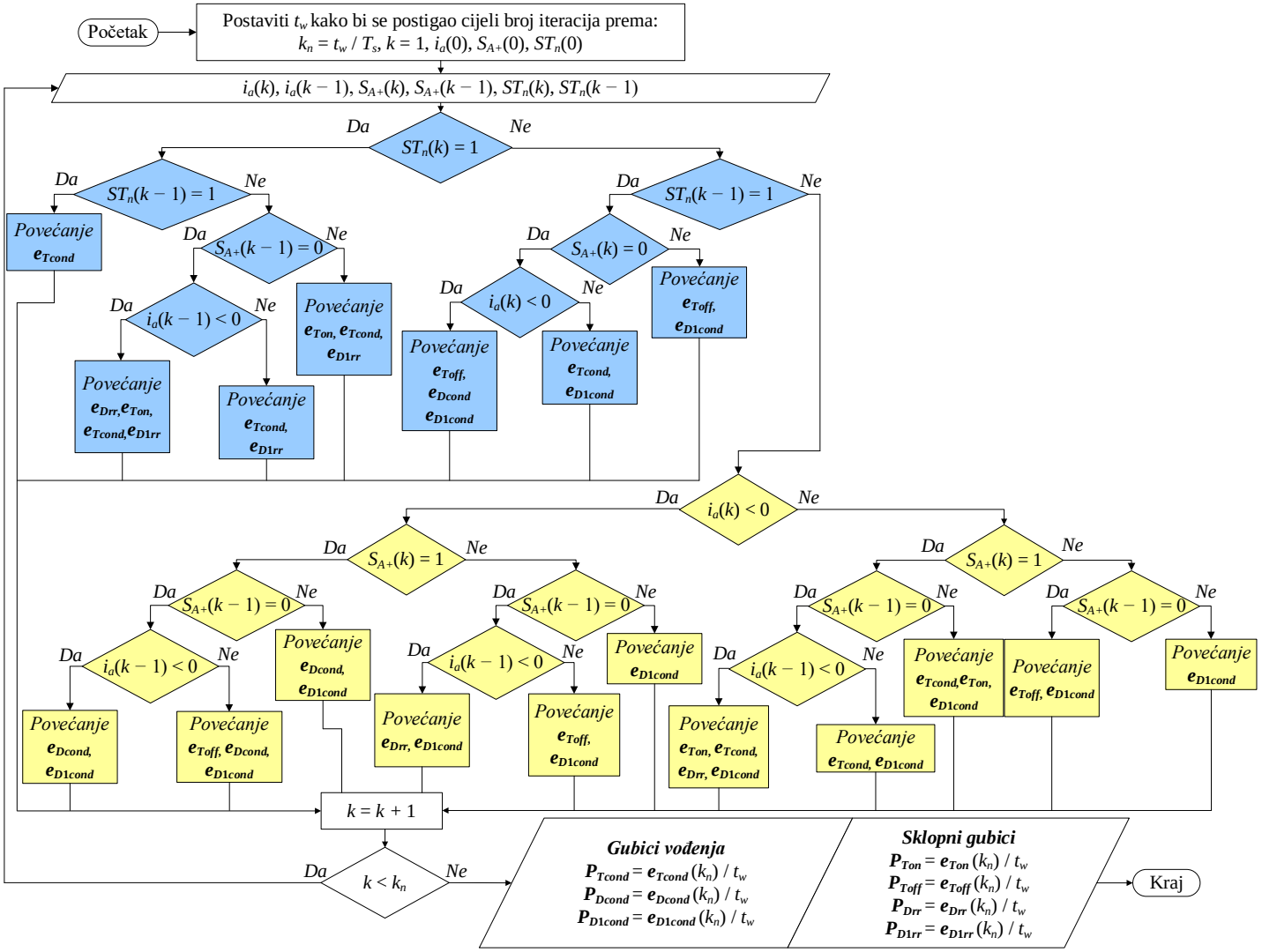
Drugi algoritam za izračun poluvodičkih gubitaka izmjenjivača kvazi Z-tipa, označen u [III] kao LCA2, utemeljen je na algoritmima koji su korišteni u [69, 70]. Poluvodički gubici računati su na temelju akumuliranih energija gubitaka u vremenu t_w, prema dijagramu toka prikazanom na slici 2.13, koji se može podijeliti u dva dijela. Plavo obojani blokovi korišteni su za izračun energije vođenja tranzistora tijekom prostrijelnog stanja te za izračun sklopnih energija tijekom promjena sklopnih stanja između aktivnih ili nultih sklopnih stanja i prostrijelnih stanja. Žuto obojani blokovi na slici 2.13 korišteni su za izračun energija gubitaka akumuliranih tijekom aktivnih i nultih sklopnih stanja. Koja će energija poluvodičkih gubitaka biti uvećana odlučuje se na temelju trenutnih vrijednosti sljedećih signala u *k*-tom i (*k* – 1)-om trenutku: upravljačkog signala S_{A+}, signala ST_n i trenutne vrijednosti fazne struje u fazi *a* (i_a). Svi signali uzorkovani su s periodom uzorkovanja T_s. Akumulirana energija vođenja tranzistora računata je na temelju trenutne vrijednosti struje kolektora (i_{ce}), prema izrazu [III]:

$$e_{Tcond}(k) = e_{Tcond}(k-1) + \left(U_{ce,0} + R_{ce}\left|i_{ce}(k)\right|\right) i_{ce}(k) \left[t(k) - t(k-1)\right] \tag{2.21}$$

Tijekom aktivnih i nultih stanja struja i_{ce} jednaka je faznoj struji i_a, dok tijekom prostrijelnog stanja vrijedi $i_{ce} = 1/2 i_a + 2/3 i_{L1}$, gdje je i_{L1} trenutna vrijednost struje kroz prigušnicu L_1.

Akumulirane energije vođenja poredne diode (e_{Dcond}) i diode u istosmjernom krugu (e_{D1cond}) izmjenjivača računate su kao:

$$\begin{aligned} e_{Dcond}(k) &= e_{Dcond}(k-1) + \left(U_{D,0} + R_D \left| i_a(k) \right| \right) i_a(k) \left[t(k) - t(k-1) \right] \\ e_{D1cond}(k) &= e_{D1cond}(k-1) + \left(U_{D1,0} + R_{D1} \left| i_{D1}(k) \right| \right) i_{D1}(k) \left[t(k) - t(k-1) \right] \end{aligned} \tag{2.22}$$

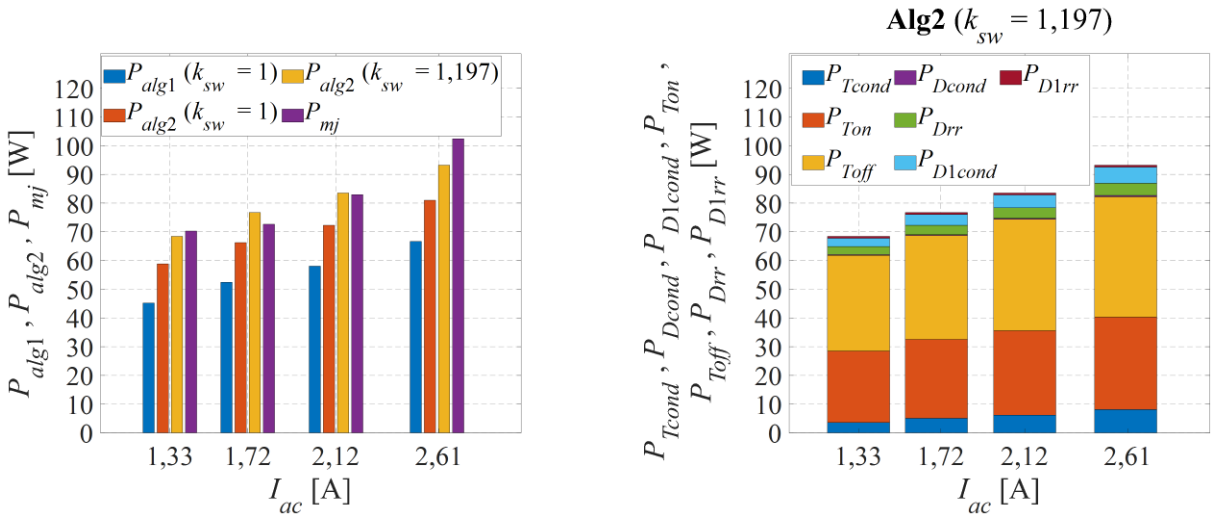


Slika 2.13. Dijagram toka drugog algoritma za izračun poluvodičkih gubitaka [III]

Akumulirane energije uklapanja (e_{Ton}) i isklapanja (e_{Toff}) tranzistora te akumulirane energije oporavljanja poredne diode (e_{Drr}) i diode u istosmjernom krugu (e_{D1rr}) računaju se kako slijedi [III]:

$$\begin{aligned} e_{Ton/off}(k) &= e_{Ton/off}(k-1) + e_{Ton/off}\left(\left|i_{ce}(k)\right|\right) \\ e_{Drr}(k) &= e_{Drr}(k-1) + e_{Drr}\left(\left|i_{a}(k)\right|\right) \\ e_{D1rr}(k) &= e_{D1rr}(k-1) + e_{D1rr}\left(\left|i_{D1}(k)\right|\right) \end{aligned} \tag{2.23}$$

Točnost oba prethodno opisana algoritma ispitana je eksperimentalno usporedbom izračunatih poluvodičkih gubitaka s izmjerenim gubicima (P_{mj}), pri čemu je $P_{mj} = P_{dc} - P_{ac} - P_L$. Izlazna snaga izmjenjivača (P_{ac}) mjerena je na izlazu izmjenjivača prije filtra valnim analizatorom Norma 4000 (Fluke), dok je ulazna snaga (P_{dc}) dobivena kao srednja vrijednost produkta struje i_{L1} i napona u_{dc}. Gubici prigušnica (P_L) računati su korištenjem postupka opisanog u [32], dok su gubici kondenzatora zanemareni zbog malog unutarnjeg otpora korištenih polipropilenskih kondenzatora (7,8 mΩ). Prvi korak u eksperimentalnoj analizi bio je odrediti faktor uvećanja sklopnih energija tranzistora (k_{sw}). To je napravljeno na temelju rezultata prikazanih na slici 2.14 gdje su izračunati gubici uspoređeni s izmjerenim za četiri različita iznosa efektivne vrijednosti fazne struje na izlazu izmjenjivača (I_{ac}): 1,33 A, 1,72 A, 2,12 A i 2,61 A. Tijekom ovih mjerenja iznos sklopne frekvencije bio je postavljen na 5 kHz, a iznos faktora D_0 na 0,22. Srednja vrijednost ulaznog napona (U_{dc}) bila je postavljena na 450 V te je, u tom slučaju, napon U_{pn} izračunat prema (1.3) iznosio približno 800 V, što je rezultiralo konstantnim omjerom napona $U_{pn}/U_{k,ref}$. Izmjenjivač je radio u otočnom načinu rada, pri čemu je efektivna vrijednost napona na trošilu bila regulirana na iznosu 230 V, a frekvencija osnovnog harmonika napona bila je postavljena na 50 Hz. Za upravljanje izmjenjivačem korištena je nova metoda utiskivanja prostrijelnog stanja s implementiranim mrtvim vremenom.



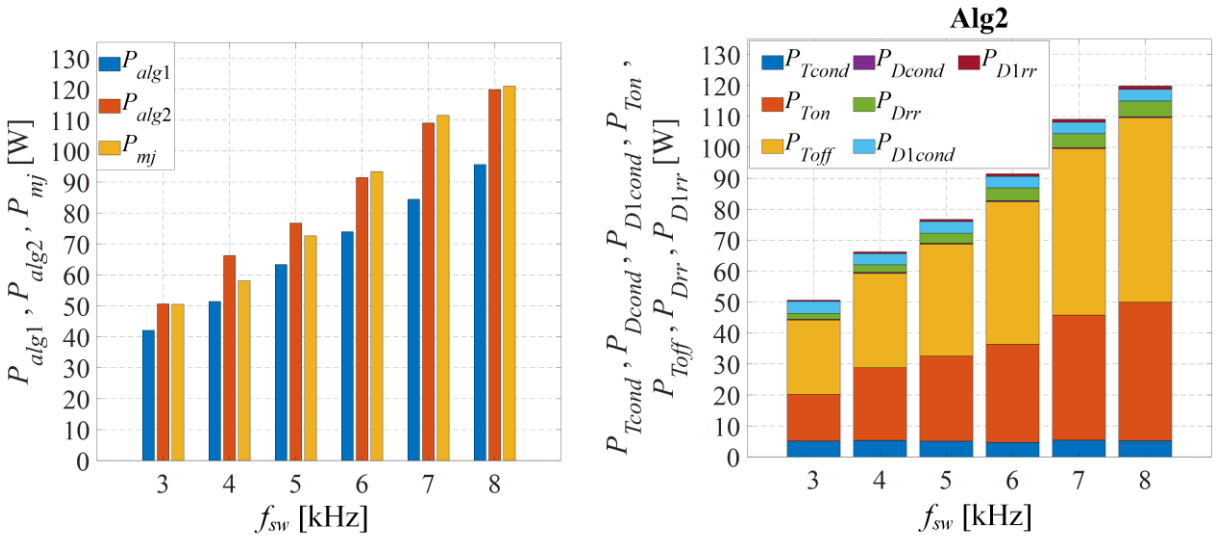
a) *b)*

Slika 2.14. Izmjereni i izračunati gubici izmjenjivača kvazi Z-tipa (a), razdioba poluvodičkih gubitaka za drugi algoritam s uračunatim faktorom k_{sw} = 1,197 (b)

Slika 2.14a prikazuje poluvodičke gubitke izračunate s prvim (P_{alg1}) i drugim (P_{alg2}) algoritmom dobivene uz jedinični faktor k_{sw} te izmjerene gubitke (P_{mj}) u ovisnosti o iznosu struje I_{ac}. Može se uočiti da je najveća apsolutna pogreška drugog algoritma od 22 W manja u odnosu na prvi algoritam kod kojeg ta pogreška iznosi 34 W. To je posljedica činjenice da drugi algoritam računa gubitke na temelju trenutnih vrijednosti mjerenih signala dok prvi algoritam računa gubitke uz određene aproksimacije npr. sinusna fazna struja. Budući da je točnost drugog algoritma bila veća, on je korišten za određivanje faktora k_{sw}. Vrijednosti faktora k_{sw} određene su za svaki od četiri razmatrana iznosa struje I_{ac} tako da se faktor k_{sw} povećavao sve dok se pogreška drugog algoritma nije svela na nulu. Za razmatrani raspon struje I_{ac}, iznos faktora k_{sw} kretao se u rasponu od 1,09 do 1,34, a konačni iznos od 1,197 dobiven je usrednjavanjem pojedinačnih iznosa. Treba napomenuti da je prilikom ovih eksperimentalnih istraživanja iznos faktora k_T bio 1,4 što je najveća preporučena vrijednost [64]. Manji iznos faktora k_T rezultirao bi većim iznosom faktora k_{sw}. Iznos faktora k_{sw} od 1,197 određen je u sklopu istraživanja provedenih pri izradi znanstvenog rada danog u prilogu A koji je objavljen u časopisu, dok je u [III] iznos faktora k_{sw} iznosio 1,53. Razlog tomu je korištenje metode sinkronizacije s nultim stanjem s izostavljenim mrtvim vremenom u [III] jer u tim istraživanjima fenomen dodatnog neželjenog naponskog pojačanja uzrokovanog neplaniranim prostrijelnim stanjima nije bio primijećen. Tako su u istraživanjima provedenim u [III] gubici nastali uslijed neplaniranih prostrijelnih stanja pripisani pogreškama sklopnih energija. Na slici 2.14a može se uočiti da se točnost drugog algoritma značajno poveća kada se uračuna faktor k_{sw} = 1,197, odnosno najveća apsolutna

pogreška se smanji na iznos od 6 W. Razdioba poluvodičkih gubitaka za drugi algoritam s uračunatim faktorom $k_{sw} = 1{,}197$ prikazana je na slici 2.14b. Gubici uklapanja (P_{Ton}) i isklapanja (P_{Toff}) tranzistora su dominantni s udjelom većim od 90 % u ukupnim poluvodičkim gubicima. Nakon toga slijede gubici vođenja tranzistora (P_{Tcond}), gubici vođenja porednih dioda (P_{Dcond}) i gubici vođenja diode u istosmjernom krugu izmjenjivača (P_{D1cond}). Gubici oporavljanja porednih dioda (P_{Drr}) i gubici oporavljanja diode u istosmjernom krugu (P_{D1rr}) imaju najmanji udio u ukupnim poluvodičkim gubicima.

Slika 2.15 prikazuje poluvodičke gubitke izračunate primjenom dvaju razmatranih algoritama s uračunatim faktorom $k_{sw} = 1{,}197$ i izmjerene poluvodičke gubitke u ovisnosti o frekvenciji f_{sw}. Tijekom ovih eksperimentalnih mjerenja struja I_{ac} iznosila je 1,72 A, napon U_{dc} iznosio je 450 V i faktor D_0 iznosio je 0,22. Izmjenjivač je radio u otočnom načinu rada pri čemu je efektivna vrijednost napona na trošilu bila regulirana na iznos od 230 V. Na slici 2.15a može se uočiti da je točnost korigiranog drugog algoritma veća od točnosti korigiranog prvog algoritma. Najveća apsolutna pogreška prvog algoritma iznosila je 25 W, dok je u slučaju drugog algoritma ta pogreška iznosila 9 W. Razdioba poluvodičkih gubitaka drugog algoritma s uračunatim faktorom $k_{sw} = 1{,}197$ prikazana je na slici 2.15b i ona odgovara razdiobi na slici 2.14b s izrazito dominantnim sklopnim gubicima tranzistora.



a) *b)*

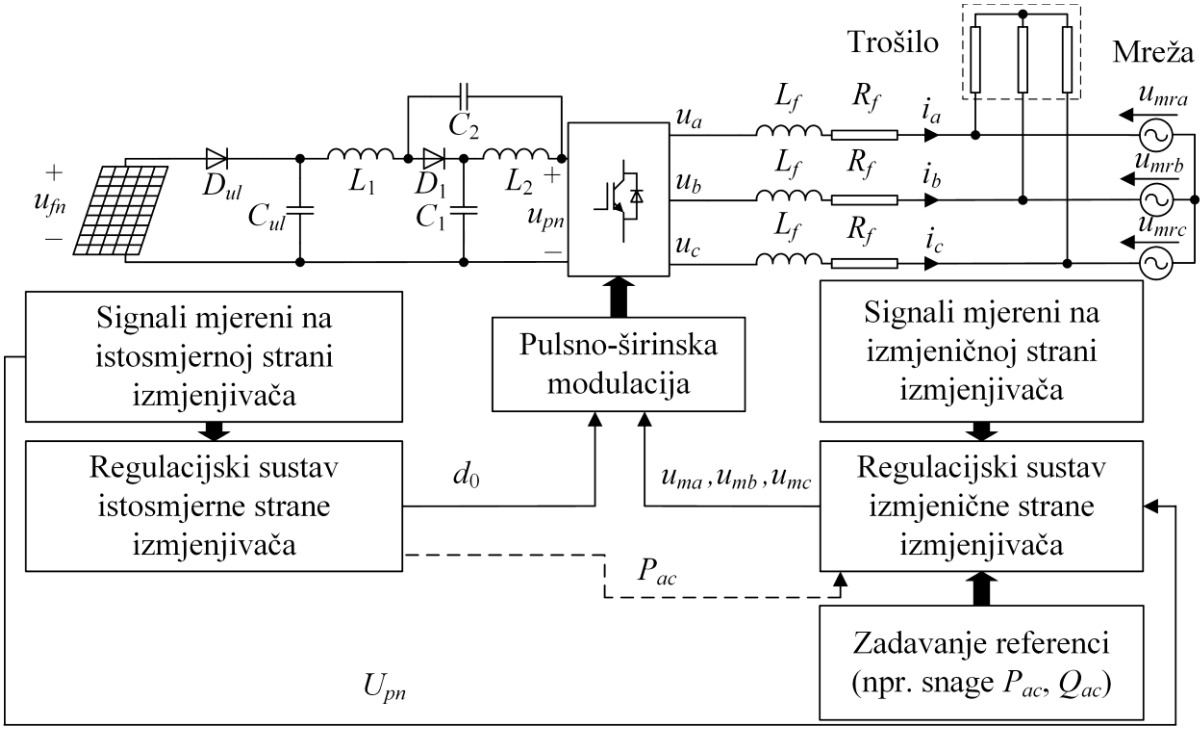
Slika 2.15. Poluvodički gubici izračunati primjenom dvaju razmatranih algoritama s uračunatim faktorom $k_{sw} = 1{,}197$ i izmjereni poluvodički gubici (a), razdioba poluvodičkih gubitaka za drugi algoritam s uračunatim faktorom k_{sw} (b)

Na kraju se može zaključiti da je poluvodičke gubitke izmjenjivača moguće odrediti sa zadovoljavajućom točnošću primjenom dvaju prethodno opisanih algoritama. Drugi algoritam

koji radi s trenutnim vrijednostima struja i napona izmjenjivača je točniji, ali je njegova implementacija složenija jer zahtijeva mjerenje više signala izmjenjivača kvazi Z-tipa. S druge strane, prvi algoritam ima manju točnost, ali je njegova implementacija jednostavnija.

3. REGULACIJSKI SUSTAVI S IZMJENJIVAČEM KVAZI Z-TIPA NAPAJANIM IZ FOTONAPONSKOG IZVORA

Izmjenjivač je osnovna komponenta u fotonaponskim sustavima koji su spojeni na izmjeničnu električnu mrežu ili služe za napajanje izmjeničnih trošila u otočnom načinu rada. Regulacijski sustav izmjenjivača regulira tok električne energije od fotonaponskog izvora prema električnoj mreži ili izmjeničnom trošilu. Načelna shema regulacijskog sustava s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora prikazana je na slici 3.1.



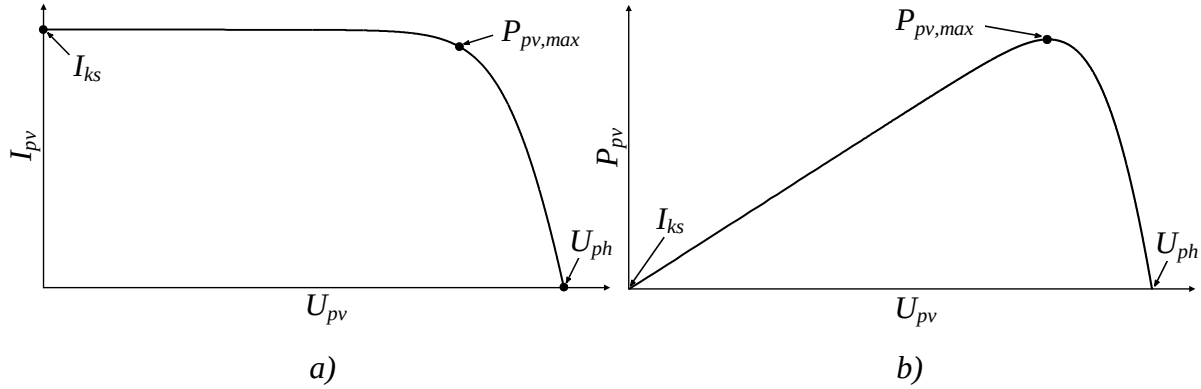
Slika 3.1. Načelna shema regulacijskog sustava s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora [25]

Fotonaponski izvor spojen na ulaz izmjenjivača sastoji se od više povezanih fotonaponskih panela najčešće spojenih u obliku fotonaponskog polja. Polje čini više paralelno spojenih nizova fotonaponskih panela, pri čemu se svaki niz sastoji od više serijski spojenih panela. Između fotonaponskog izvora i ulaza u izmjenjivač najčešće se postavlja dioda (D_{ul} na slici 3.1) koja sprječava tok struje natrag u fotonaponski izvor. Kondenzator C_{ul} na slici 3.1 služi za filtriranje ulaznog napona izmjenjivača. Regulacijski sustav na slici 3.1 sastoji se od regulacijskog sustava istosmjerne i izmjenične strane. Osnovna zadaća regulacijskog sustava izmjenične strane je regulacija napona trošila u otočnom načinu rada ili regulacija snage u točki priključka na mrežu u spoju s mrežom. Otočni način rada sustava prikazanog na slici 3.1 razmatran u [11, 29, 71] nije od posebnog značaja jer je u tom načinu rada praktički

nemoguće osigurati rad fotonaponskog izvora u točki maksimalne snage zbog toga što snaga koja se dobije iz fotonaponskog izvora mora uvijek odgovarati zbroju snage na trošilu i gubitaka izmjenjivača. U spoju s mrežom, regulacijski sustav izmjenične strane zahtijeva mjerenje struja koje teku od izmjenjivača prema mreži, mjerenje napona mreže i mjerenje napona na istosmjernoj strani izmjenjivača. Izlazni signali regulacijskog sustava izmjenične strane u pravilu su modulacijski signali. Regulacijski sustav istosmjerne strane ima zadaću osigurati rad fotonaponskog izvora u točki maksimalne snage u spoju s mrežom. Izlazni signal ovog sustava je, u većini slučajeva, faktor D_0, a u nekim aplikacijama izlazni signal je referenca radne snage (P_{ac}) za regulacijski sustav izmjenične strane izmjenjivača. U nastavku su analizirane nadomjesne sheme fotonaponskog izvora, s naglaskom na shemu predloženu u [I], i karakteristični regulacijski sustavi s izmjenjivačem kvazi Z-tipa, s naglaskom na sustav predložen u [II].

3.1. Nadomjesne sheme i karakteristike fotonaponskog izvora

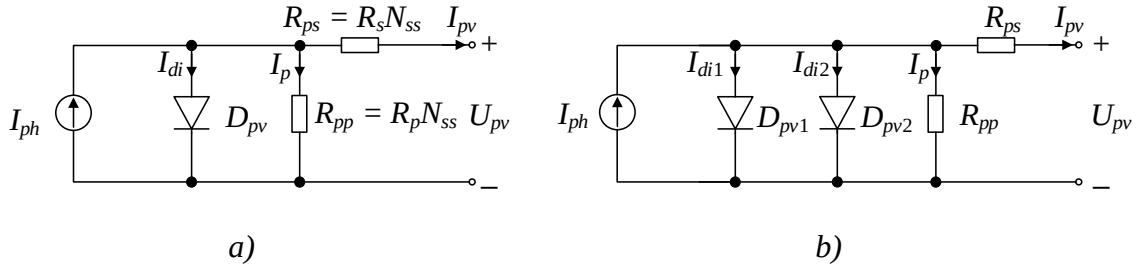
Fotonaponski izvor pretvara energiju sunčeva zračenja izravno u električnu energiju. Ta pretvorba događa se u fotonaponskoj ćeliji, koja se sastoji od dva ili više tankih slojeva poluvodičkog materijala, najčešće silicija. Kada se fotonaponska ćelija izloži sunčevom zračenju, poteče istosmjerna električna struja. Snaga jedne ćelije je mala pa se u pravilu više ćelija veže serijski, čime se dobije fotonaponski panel. Strujno-naponska karakteristika panela je nelinearna, što je posljedica činjenice da su ćelije koje čine fotonaponski panel izrađene od poluvodičkih materijala. Slika 3.2a prikazuje ovisnost struje fotonaponskog panela (I_{pv}) o naponu panela (U_{pv}). Na krivulji su označeni napon praznog hoda (U_{ph}), struja kratkog spoja (I_{ks}) te točka maksimalne snage ($P_{pv,max}$).



Slika 3.2. Karakteristike fotonaponskog panela: ovisnost struje o naponu (a), ovisnost snage o naponu (b)

Na temelju karakteristike dane na slici 3.2a moguće je dobiti karakteristiku koja prikazuje ovisnost snage fotonaponskog panela (P_{pv}) o naponu U_{pv}, koja je prikazana na slici 3.2b.

Modeliranje nelinearne strujno-naponske karakteristike fotonaponskog panela podrazumijeva odabir odgovarajuće nadomjesne sheme. Dva najzastupljenija modela fotonaponskog panela prikazana su na slici 3.3. Model s jednom diodom [72-78], prikazan na slici 3.3a, najčešće je korišten model u literaturi. Sastoji se od strujnog izvora, povratne diode (D_{pv}) te serijski i paralelno spojenog otpornika. Serijski otpor panela (R_{ps}) i paralelni otpor panela (R_{pp}) su N_{ss} puta veći u odnosu na serijski (R_s) i paralelni (R_p) otpor jedne ćelije, gdje je N_{ss} broj serijski spojenih ćelija unutar panela. Dodavanjem još jedne diode u model s jednom diodom dobije se model s dvije diode [79-83], prikazan na slici 3.3b. Prednost modela s dvije diode u odnosu na model s jednom diodom je veća točnost u području nižih osunčanosti i temperatura. To je potvrđeno u eksperimentalnim istraživanjima provedenim u [I] gdje su uspoređene izmjerene strujno-naponske karakteristike s karakteristikama dobivenim primjenom dvaju spomenutih modela. Zbog toga je u nastavku analize težište na modelu s dvije diode.



a) *b)*

Slika 3.3. Nadomjesna shema fotonaponskog panela s jednom diodom (a) i s dvije diode (b)

Struja fotonaponskog panela u modelu s dvije diode, dobivena na temelju nadomjesne sheme na slici 3.3b, izračunava se kako slijedi [79-83], [I]:

$$I_{pv} = I_{ph} - I_{di1} - I_{di2} - I_p$$

$$I_{pv} = I_{ph} - I_{01}\left(e^{\frac{q\left(U_{pv}+I_{pv}R_{ps}\right)}{a_1 kT}} - 1\right) - I_{02}\left(e^{\frac{q\left(U_{pv}+I_{pv}R_{ps}\right)}{a_2 kT}} - 1\right) - \frac{U_{pv}+I_{pv}R_{ps}}{R_{pp}} \qquad (3.1)$$

gdje je:

I_{ph} struja strujnog izvora

I_{01} reverzna struja zasićenja diode D_{pv1}, odnosno struja koja teče u odsustvu svjetlosti

I_{02} reverzna struja zasićenja diode D_{pv2}

a_1 faktor idealnosti diode D_{pv1}

a_2 faktor idealnosti diode D_{pv2}

q naboj elektrona ($1{,}6 \cdot 10^{-19}$ C)

k Boltzmannova konstanta ($1{,}38 \cdot 10^{-23}$ J/K)

T trenutna temperatura panela

Utjecaj promjene osunčanosti na karakteristiku panela uračunava se u izrazu za struju I_{ph}, koja se računa prema izrazu [75, 76, 78]:

$$I_{ph} = \frac{Z}{Z_n}\left[I_{ks} + K_i\left(T - T_n\right)\right] \tag{3.2}$$

gdje je:

Z trenutna osunčanost panela

Z_n nazivna osunčanost panela (obično 1000 W/m^2)

K_i faktor promjene struje uslijed promjene temperature

T_n nazivna temperatura panela (obično 25 ˚C)

Utjecaj promjene temperature na karakteristiku fotonaponskog panela uračunava se u izrazima koji definiraju iznose struja dioda. Posebno su važne struje zasićenja, koje se računaju kao [83], [I]:

$$\begin{aligned} I_{01} &= \frac{I_{ks} + K_i\left(T - T_n\right)}{e^{\frac{q\left(U_{ph} + K_v\left(T - T_n\right)\right)}{N_{ss} a_1 k T_n}} - 1} \\ I_{02} &= \frac{\left(T\right)^{\frac{2}{5}}}{3{,}77} I_{01} \end{aligned} \tag{3.3}$$

gdje je K_v faktor promjene napona uslijed promjene temperature panela.

Prethodno spomenuti modeli fotonaponskog panela s jednom i dvije diode spadaju u statičke modele jer ne opisuju dinamička svojstva panela. Modeli koji opisuju ova svojstva nazivaju se dinamički modeli i oni se dobiju dodavanjem odgovarajućih kapaciteta dioda u statički model. U [84], dinamika je modelirana dodavanjem promjenjivog difuzijskog kapaciteta u model s jednom diodom, dok je u [85] isto napravljeno dodavanjem eksperimentalno određenog kapaciteta osiromašenog područja u isti model. S druge strane, u [86] je dinamika modelirana dodavanjem promjenjivog kapaciteta osiromašenog područja i promjenjivog difuzijskog kapaciteta u model s jednom diodom. U [87], ova dva promjenjiva

kapaciteta dodana su u model s dvije diode. To znači da iako se u [87] radi o modelu s dvije diode, dinamika je uračunata kao da se radi o modelu s jednom diodom.

Slika 3.4 prikazuje nadomjesnu shemu dinamičkog modela fotonaponskog panela s dvije diode, koji je predložen u [I]. Dinamika je modelirana dodavanjem promjenjivog difuzijskog kapaciteta i promjenjivog kapaciteta osiromašenog područja zasebno za svaku od dioda. To znači da su u nadomjesnu shemu fotonaponskog panela dodana četiri kondenzatora s promjenjivim kapacitetima. Difuzijski kapacitet diode posljedica je postojanja manjinskih nosioca naboja u blizini prijelaznog područja PN spoja. Ovaj kapacitet je dominantan kad je dioda u stanju vođenja i povećava se sa strujom vođenja prema izrazu [I]:

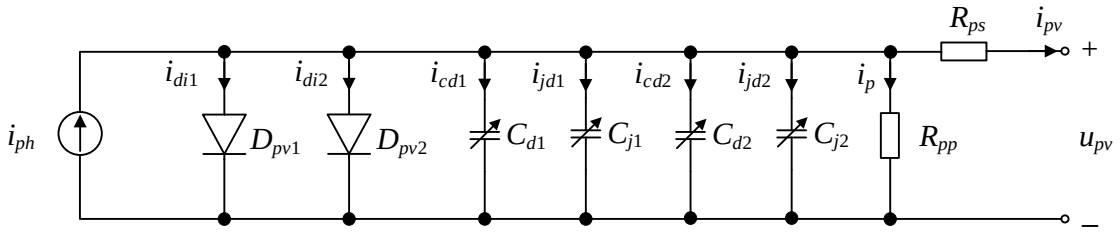
$$C_{d1/2}\left(T,u_{pv},i_{pv}\right)=\frac{q\tau I_{di1/2}\left(T,u_{pv},i_{pv}\right)}{akTN_{ss}} \tag{3.4}$$

gdje τ predstavlja srednje vrijeme života manjinskih nosioca naboja.

Kapacitet osiromašenog područja diode posljedica je elektrona i šupljina koji postoje u osiromašenom području PN spoja. Ovaj kapacitet dominantan je za male iznose propusnog napona, a definira se kao [I]:

$$C_{j1/2}\left(u_{pv},i_{pv}\right)=\frac{C_{j0}}{N_{ss}\sqrt{1-\frac{u_{pv}-i_{pv}R_{ps}}{\varphi_0 N_{ss}}}} \tag{3.5}$$

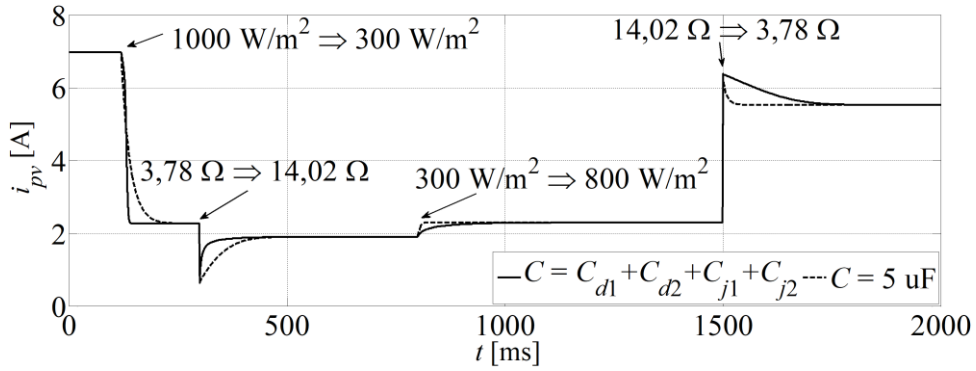
gdje je φ_0 kontaktni potencijal PN spoja, a C_{j0} je kapacitet osiromašenog područja pri kontaktnom potencijalu PN spoja φ_0; oba navedena parametra ovise o materijalu od kojeg su izrađene ćelije fotonaponskog panela.



Slika 3.4. Nadomjesna shema fotonaponskog panela s dvije diode i promjenjivim kapacitetima dioda [I]

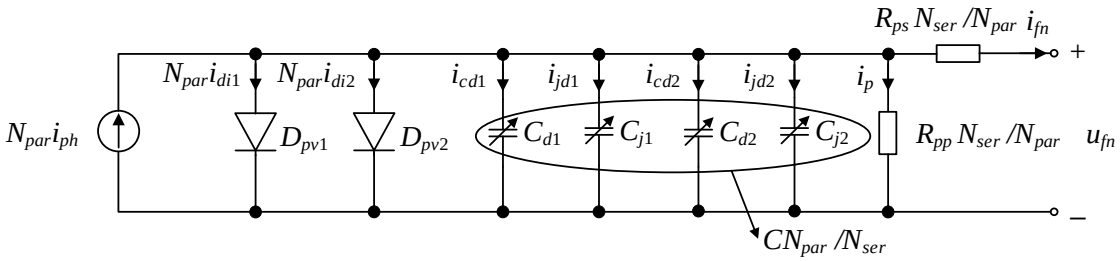
U [I], na temelju nadomjesne sheme sa slike 3.4 izrađen je simulacijski model fotonaponskog panela SV60-235E (Solvis) korištenjem programskog paketa Matlab Simulink. U simulacijskim ispitivanjima novi model fotonaponskog panela s dvije diode i

promjenjivim kapacitetima dioda uspoređen je s postojećim modelom s dvije diode i jednim konstantnim kapacitetom, čiji je iznos od 5 μF u [88] određen eksperimentalno. Simuliran je rad fotonaponskog panela izravno spojenog na radno trošilo, pri skokovitim promjenama osunčanosti i otpora radnog trošila. Rezultati simulacije prikazani na slici 3.5 ukazuju na to da postoje značajne razlike u odzivu struje panela između modela s promjenjivim i konstantnim kapacitetima. Primjetno je da je dinamika promjene struje panela brža tijekom skokovitih promjena opterećenja kada se primjenjuje model s promjenjivim kapacitetima i kada osunčanost iznosi 300 W/m^2. Suprotno tome, kada osunčanost iznosi 800 W/m^2 onda je dinamika promjene struje panela brža kada se koristi model s konstantnim kapacitetima. To je i očekivano s obzirom na to da kapacitet u modelu s promjenjivim kapacitetima, pogotovo difuzijski koji je dominantan, ovisi o struji fotonaponskog panela, koja se mijenja s promjenom osunčanosti prema izrazu (3.2).



Slika 3.5. Odziv struje fotonaponskog panela pri skokovitim promjenama osunčanosti i otpora trošila za dva razmatrana dinamička modela panela [I]

Nadomjesnu shemu fotonaponskog izvora koji se sastoji od više međusobno spojenih fotonaponskih panela moguće je dobiti na temelju nadomjesne sheme jednog panela. Slika 3.6 prikazuje nadomjesnu shemu fotonaponskog izvora koji se sastoji od N_{par} paralelno spojenih nizova fotonaponskih panela, pri čemu se svaki niz sastoji od N_{ser} serijski spojenih panela [II]. Ovakvim spajanjem postiže se N_{ser} puta veći napon fotonaponskog izvora (u_{fn}) u odnosu na napon jednog panela (u_{pv}) te N_{par} puta veća struja izvora (i_{fn}) u odnosu na struju jednog panela (i_{pv}). Bitno je naglasiti da nadomjesna shema prikazana na slici 3.6 vrijedi uz pretpostavku zanemarenog efekta zasjenjenja pojedinih panela koji čine fotonaponski izvor.



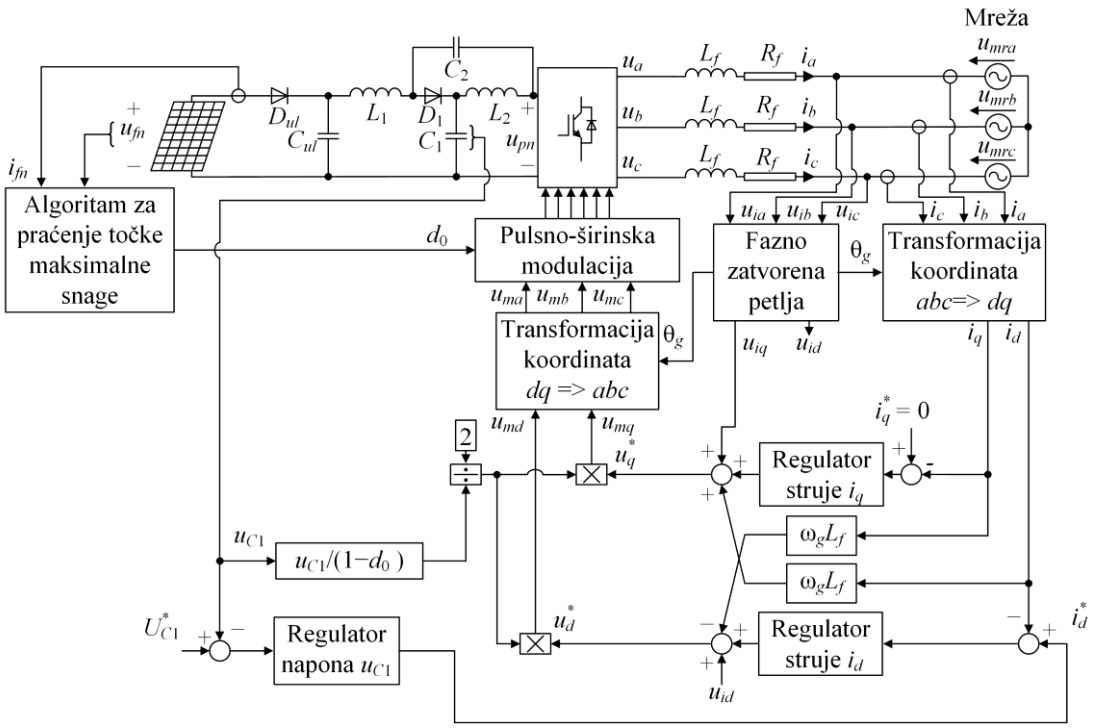
Slika 3.6. Nadomjesna shema fotonaponskog izvora koji se sastoji od N_{par} paralelno spojenih nizova panela sastavljenih od N_{ser} serijski spojenih panela [II]

3.2. Regulacijski sustavi s izmjenjivačem kvazi Z-tipa spojenim na električnu mrežu

Izmjenjivač kvazi Z-tipa u fotonaponskim sustavima najčešće se koristi za povezivanje fotonaponskog izvora s izmjeničnom električnom mrežom [10, 12-23], [II]. Zadaci regulacijskog sustava s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora u spoju s električnom mrežom su osiguravanje rada izvora u točki maksimalne snage i regulacija struja koje teku od izmjenjivača prema mreži. Ovi regulacijski sustavi mogu biti izvedeni u stacionarnom (αβ) koordinatnom sustavu [15, 18, 20, 21] ili sinkrono rotirajućem (*dq*) koordinatnom sustavu [10, 12, 13, 19, 22, 23]. Prednost realizacije regulacijskog sustava u αβ koordinatnom sustavu u odnosu na *dq* sustav je niži udio viših harmonika u izlaznim strujama izmjenjivača. Međutim, sinteza regulacijskog sustava je složenija u αβ sustavu zbog korištenja proporcionalno-rezonantnih regulatora, dok je u *dq* koordinatnom sustavu moguće koristiti klasične proporcionalno-integracijske (PI) i proporcionalno-integracijsko-derivacijske (PID) regulatore. Osnovna karakteristika regulacijskih sustava realiziranih u *dq* koordinatnom sustavu je mogućnost regulacije radne i jalove snage koje se injektiraju u električnu mrežu regulacijom *d* i *q* komponenti vektora struje mreže, slijedom. To se najčešće osigurava implementacijom fazno zatvorene petlje [89] koja osigurava sinkronizaciju vektora napona na izlazu izmjenjivača s vektorom napona mreže uz kompenzaciju utjecaja filtra na izlazu izmjenjivača.

Slike 3.7 i 3.8 prikazuju dva karakteristična regulacijska sustava realizirana u *dq* koordinatnom sustavu s izmjenjivačem kvazi Z-tipa u spoju s električnom mrežom i napajanim iz fotonaponskog izvora. U regulacijskom sustavu prikazanom na slici 3.7, referenca *d*-komponente vektora struje mreže (i_d^*) dobivena je na izlazu regulatora napona na kondenzatoru C_1 (u_{C1}), dok je praćenje točke maksimalne snage fotonaponskog izvora osigurano promjenom faktora d_0. S druge strane, u regulacijskom sustavu prikazanom na

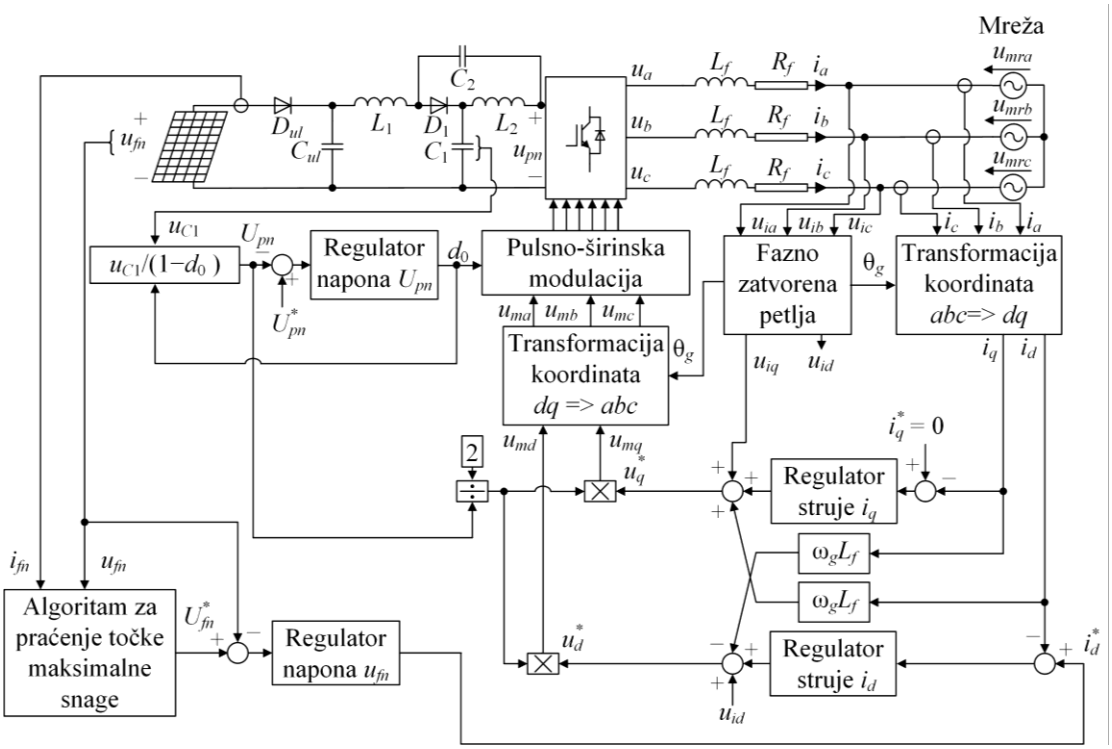
slici 3.8 napravljeno je suprotno, pri čemu nije reguliran napon u_{C1} nego napon na ulazu u most izmjenjivača (u_{pn}), koji je računat na temelju mjerenog napona u_{C1}. Za realizaciju oba razmatrana regulacijska sustava potrebno je mjerenje triju veličina u istosmjernom krugu izmjenjivača: napona (u_{fn}) i struje (i_{fn}) fotonaponskog izvora i napona u_{C1}. U regulacijskom sustavu predloženom u [12] korištene su prijenosne funkcije kako bi se procijenili iznosi napona u_{fn} i u_{C1} te time izbjegla potreba za njihovim mjerenjem. Točnost prijenosnih funkcija zadovoljavajuća je u blizini točke linearizacije, no značajno se smanjuje odmicanjem od te točke, što dovodi u pitanje rad ovakvog sustava u radnim točkama koje su daleko od točke linearizacije.



Slika 3.7. Regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora u kojemu se točka maksimalne snage prati promjenom faktora d_0 [19]

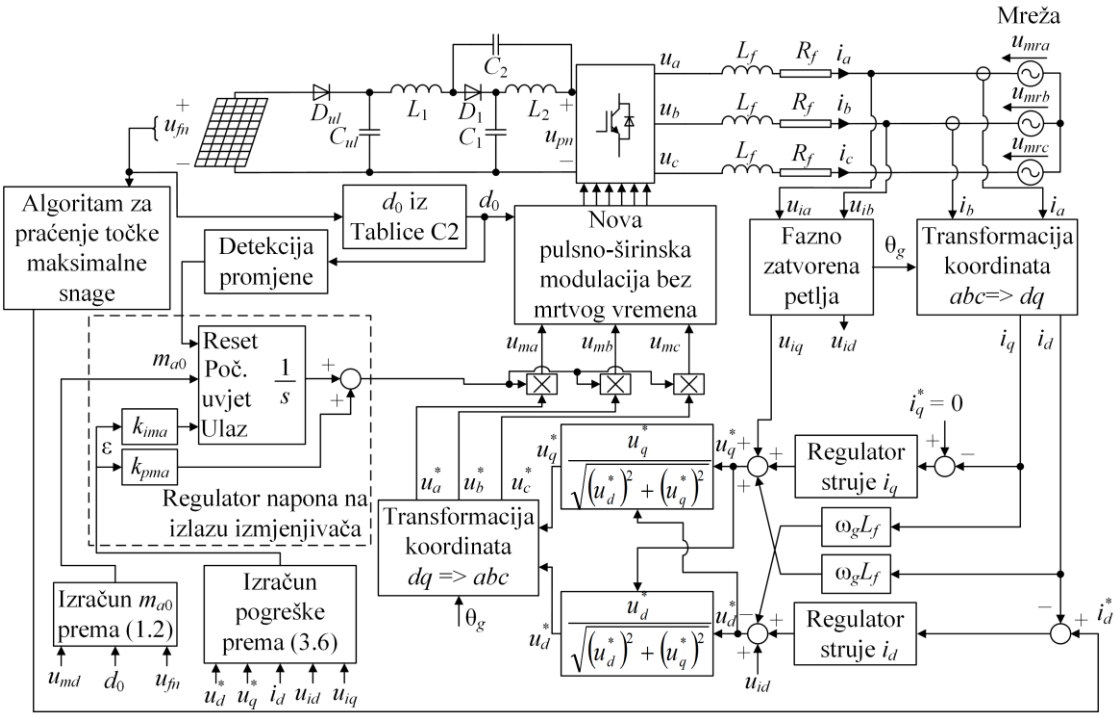
U regulacijskim sustavima prikazanim na slikama 3.7 i 3.8, *d* i *q* komponente vektora struje mreže (i_d i i_q), dobiju se transformacijom faznih struja (i_a, i_b, i_c). Kut θ_g potreban za transformacije dobiva se iz fazno zatvorene petlje kao izlaz regulatora koji regulira *q*-komponentu vektora napona (u_{iq}) na nulu, dok je odgovarajuća *d*-komponenta vektora napona jednaka vršnoj vrijednosti osnovnog harmonika mrežnog napona ($u_{id} = \hat{U}_m$). Rasprezanje između osi *d* i *q* izvedeno je dodavanjem odgovarajućeg člana $\omega_g L_f$, gdje ω_g predstavlja kružnu frekvenciju mreže koja se dobiva iz fazno zatvorene petlje, a L_f predstavlja

induktivitet L filtra. U oba razmatrana regulacijska sustava referenca *q*-komponente vektora struje mreže (i_q^*) postavljena je na nulu kako se u mrežu ne bi injektirala jalova snaga.



Slika 3.8. Regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora u kojemu se točka maksimalne snage prati promjenom d-komponente vektora struje mreže [23]

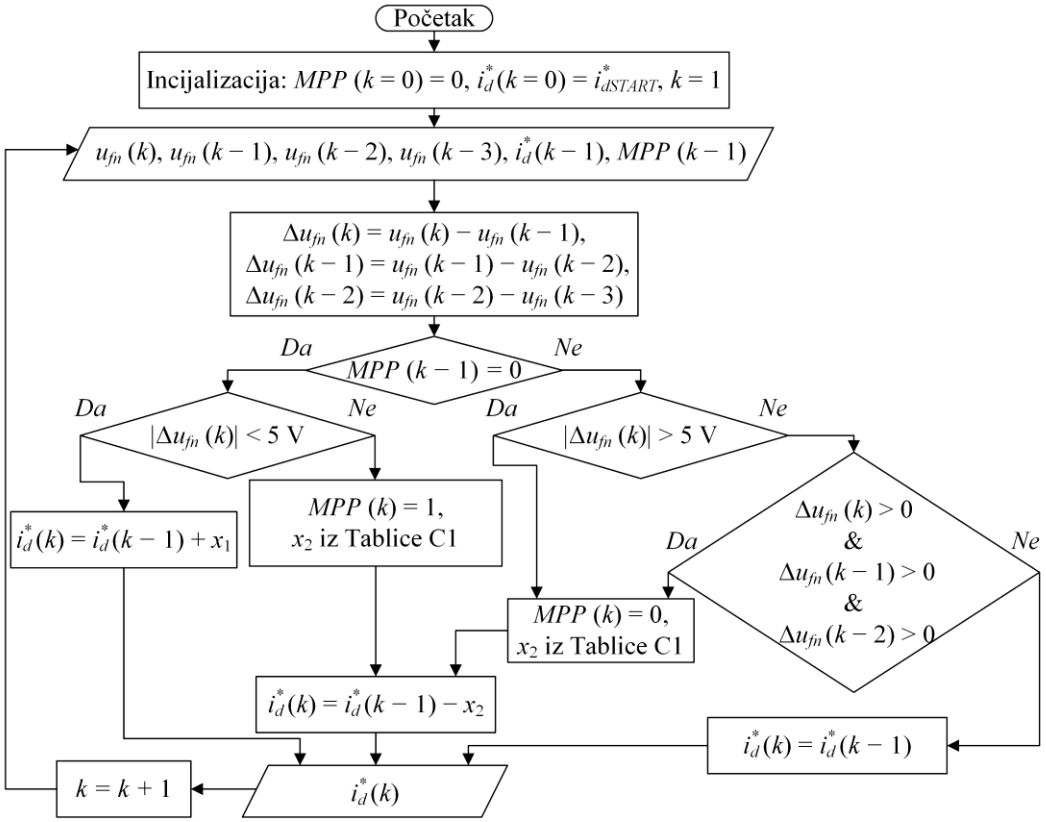
Slika 3.9 prikazuje regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora i spojenim na električnu mrežu, kakav je predložen u [II].



Slika 3.9. Regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora kakav je predložen u [II]

Regulacijski sustav prikazan na slici 3.9 realiziran je u *dq* koordinatnom sustavu, pri čemu je struja i_q^* postavljena u nulu kako bi se osigurao jedinični faktor snage. Za upravljanje izmjenjivačem kvazi Z-tipa korištena je nova pulsno-širinska modulacija kod koje je početak prostrijelnog stanja sinkroniziran s početkom nultog sklopnog stanja. Bitno je naglasiti da mrtvo vrijeme nije bilo implementirano u upravljačke signale tranzistora jer u toj fazi istraživanja još nije bilo uočeno postojanje neželjenih prostrijelnih stanja. Osim toga, rad novog regulacijskog sustava ispitan je isključivo na simulacijskoj razini pa mrtvo vrijeme nije ni bilo potrebno uvoditi jer su tranzistori modelirani kao idealne sklopke.

Zadatak razmatranog regulacijskog sustava je praćenje točke maksimalne snage, što je u [II] postignuto implementacijom novog algoritma čiji je dijagram toka prikazan na slici 3.10. Ulazne veličine u algoritam su iznosi napona u_{fn} u *k*-tom, $(k-1)$-om, $(k-2)$-om i $(k-3)$-em trenutku, dok je izlazna veličina iznos struje i_d^*.



Slika 3.10. Dijagram toka algoritma za praćenje točke maksimalne snage koji je predložen u [II]

Predloženi algoritam prati točku maksimalne snage uz pretpostavku da se u području koje se na $I_{pv} - U_{pv}$ i $P_{pv} - U_{pv}$ karakteristikama prikazanim na slici 3.2 nalazi desno od točke maksimalne snage ($P_{pv,max}$) za male promjene napona fotonaponskog izvora događaju velike promjene struje izvora. S druge strane, na dijelu karakteristika koji se nalazi lijevo od točke maksimalne snage, za velike promjene napona događaju se male promjene struje. U sustavu koji je prikazan na slici 3.9, radna točka fotonaponskog izvora mijenja se skokovitom promjenom iznosa struje i_d^* pri čemu se praćenjem promjene iznosa napona u_{fn} (Δu_{fn}) zaključuje na kojem se dijelu karakteristike nalazi radna točka. Iznos struje i_d^* se iz koraka u korak uvećava za x_1 (x_1 = 0,1 A u [II]) sve dok se ne detektira da je radna točka prešla u područje lijevo od točke maksimalne snage. Prijelaz radne točke lijevo od točke maksimalne snage detektira se kada je apsolutna vrijednost promjene Δu_{fn} veća od 5 V. Nakon detekcije prijelaza, struja i_d^* umanji se za iznos x_2 dobiven na temelju iznosa Δu_{fn} iz tablice C1 (prilog C) i signal *MPP* (od engl. *maximum power point*) se postavi u jedinicu. Signal *MPP* predstavlja logički signal koji ima vrijednost 0 kada nije postignuta točke maksimalne snage i vrijednost 1 kada se smatra da je točka maksimalne snage postignuta. Kada je *MPP* = 1, iznos struje i_d^* se ne mijenja sve dok se ne detektira promjena osunčanosti ili temperature

fotonaponskog izvora. Za konstantni iznos struje i_d^* promjena osunčanosti i/ili temperature fotonaponskog izvora uzrokuje promjenu snage p_{fn}. Ta promjena snage uzrokuje promjenu napona u_{fn} na temelju čije promjene se detektira promjena osunčanosti/temperature. Kada se detektira ova promjena, signal *MPP* postavlja se u nulu, a struja i_d^* umanji se za iznos x_2 dobiven iz tablice C1 (prilog C) te se u sljedećim koracima ponovno traži točka maksimalne snage.

Korištenje prethodno opisanog algoritma za praćenje točke maksimalne snage osigurava praćenje točke maksimalne snage bez oscilacija i bez mjerenja struje fotonaponskog izvora. Nadalje, u regulacijskom sustavu prikazanom na slici 3.9 koristi se i PI regulator napona na izlazu izmjenjivača koji ima odgovarajuće proporcionalno pojačanje (k_{pma}) i integracijsko pojačanje (k_{ima}). Signal pogreške ovog regulatora računa se na temelju vektorskog dijagrama izmjenične strane izmjenjivača te je definiran kako slijedi:

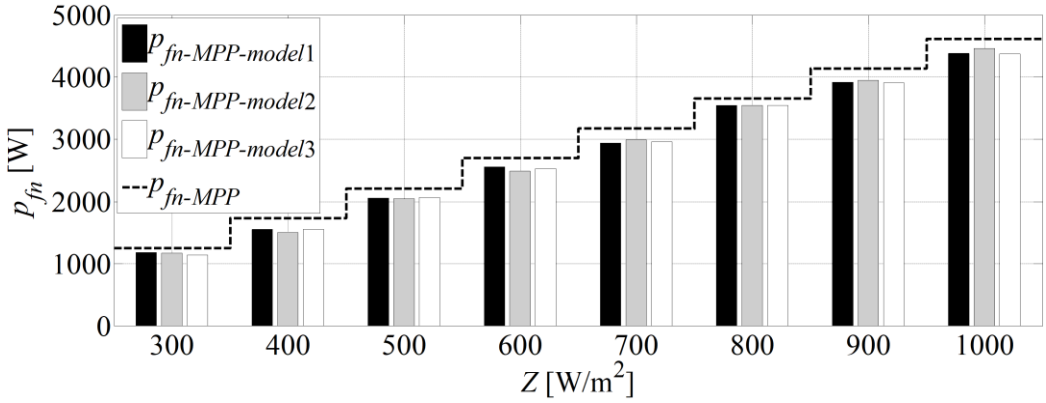
$$\varepsilon = \sqrt{\left(u_d^*\right)^2 + \left(u_q^*\right)^2} - \sqrt{\left(u_{id}\right)^2 + \left(u_{iq}\right)^2 + \left(i_d \omega_g L_f\right)^2} \tag{3.6}$$

Signal pogreške ε računa se na temelju referentnih napona u *dq* koordinatnom sustavu u_d^* i u_q^*, napona u_{id} i u_{iq}, koji se dobiju iz fazno zatvorene petlje, te struje i_d. Konačno, implementacija novog algoritma za praćenje točke maksimalne snage i regulatora napona na izlazu izmjenjivača u [II] ne zahtijeva senzore struje fotonaponskog izvora i napona u_{C1}, koji su nužni za rad regulacijskih sustava predloženih u literaturi.

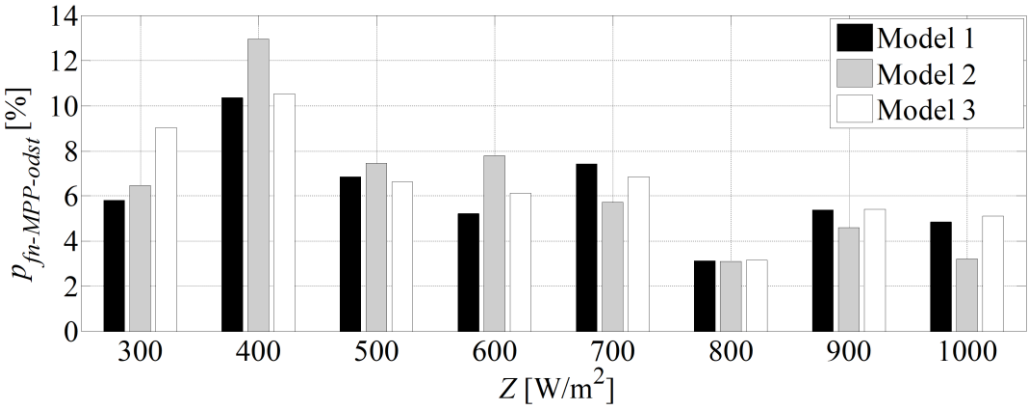
Promjena temperature fotonaponskog izvora uzrokuje osjetnu promjenu napona fotonaponskog izvora. Iznos faktora d_0 mijenja se s obzirom na iznos napona u_{fn} prema tablici C2 (prilog C) kako bi se osiguralo dovoljno pojačanje napona u_{fn}. Skokovita promjena faktora d_0 dovodi to prijelazne pojave u naponu na izlazu izmjenjivača. Kako bi se ta prijelazna pojava ublažila, početna vrijednost indeksa amplitudne modulacije promijeni se na iznos m_{a0}, koji se računa na temelju jednadžbe (1.2), svaki put kada se faktor d_0 promijeni. To znači da se integrator PI regulatora napona na izlazu izmjenjivača resetira svaki put kada se faktor d_0 promijeni.

Rad regulacijskog sustava prikazanog na slici 3.9 ispitan je primjenom simulacijskog modela izrađenog u programskom paketu Matlab Simulink, uz primjenu isključivo osnovnih Simulink blokova. Dodatni cilj ispitivanja je bio provjeriti ovisi li rad regulacijskog sustava o modelu fotonaponskog izvora. Razmatrane su statičke i dinamičke karakteristike sustava za različite osunčanosti i temperature fotonaponskog izvora s naglaskom na učinkovitost

praćenja točke maksimalne snage. U nastavku su dani najznačajniji rezultati, dok je ostatak rezultata dostupan u [II]. Slika 3.11a prikazuje ovisnost snage fotonaponskog izvora o osunčanosti izvora, dok slika 3.11b prikazuje postotno odstupanje od točke maksimalne snage za tri različita modela izvora u ovisnosti o osunčanosti za temperaturu panela od 75 ˚C. Prvi model izvora (model 1) je statički model s dvije diode, drugi model (model 2) je dinamički model s promjenjivim kapacitetima iz [I] i treći model (model 3) je dinamički model s konstantnim kapacitetom. Slika 3.11a prikazuje da se maksimalne snage $p_{fn\text{-}MPP}$ dobivene za tri razmatrana modela međusobno razlikuju te da postoji odstupanje sve tri od stvarne maksimalne snage (isprekidana crta).



a)

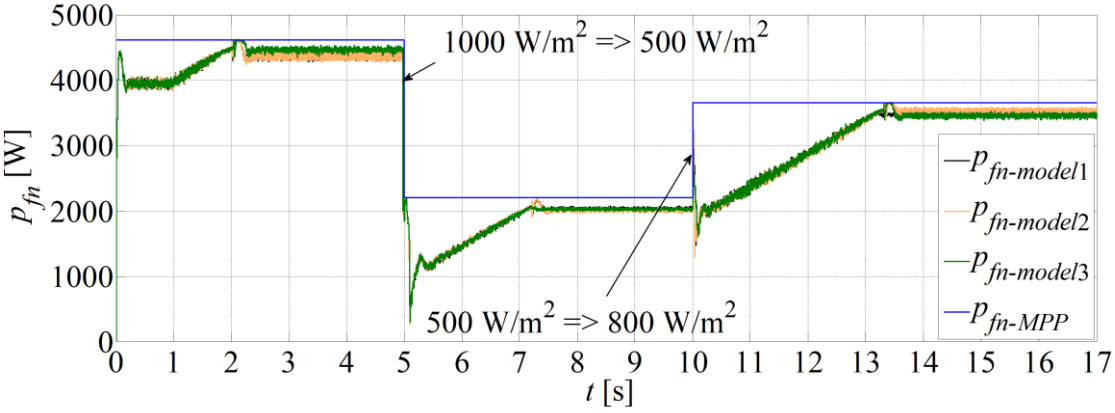


b)

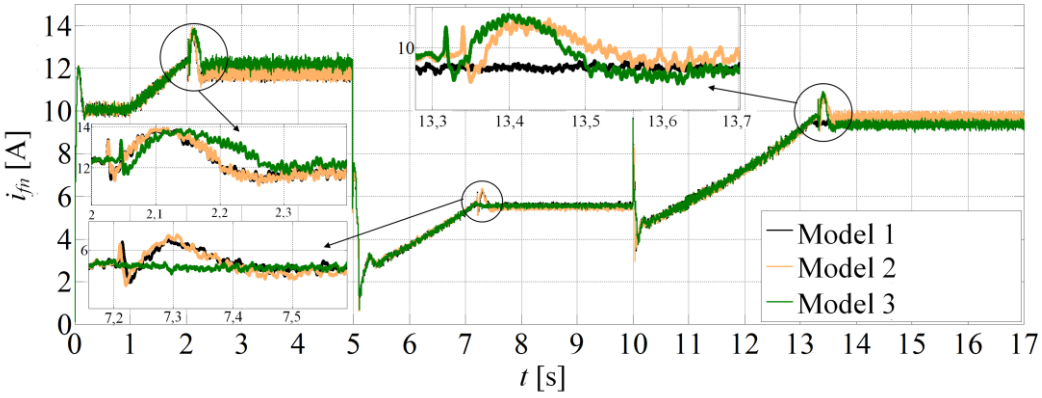
Slika 3.11. Usporedba modela fotonaponskog izvora: snaga fotonaponskog izvora u ovisnosti o osunčanosti (a), postotno odstupanje od točke maksimalne snage (b) [II]

Za postotno odstupanje od točke maksimalne snage ($p_{fn\text{-}MPP\text{-}odst}$) prikazano na slici 3.11b može se reći da se smanjuje s porastom osunčanosti te da ovisi o korištenom modelu fotonaponskog izvora. Razlike između modela fotonaponskog izvora postoje praktički za sve razmatrane osunčanosti.

Slika 3.12 prikazuje dinamičke odzive snage fotonaponskog izvora (a) i struje fotonaponskog izvora (b) pri skokovitim promjenama osunčanosti izvora i temperaturi panela od 75 ˚C. U prvoj sekundi uključen je algoritam za praćenje točke maksimalne snage te je maksimalna snaga dostignuta u drugoj sekundi. U t = 5 s nastupa skokovita promjena iznosa osunčanosti s 1000 W/m^2 na 500 W/m^2. U algoritmu se detektira promjena osunčanosti te se pokreće ponovno praćenje točke maksimalne snage koja je dostignuta u približno sedmoj sekundi kada je struja i_d^* postavljena na konstantnu vrijednost. Nova skokovita promjena osunčanosti u 10. sekundi na iznos od 800 W/m^2 detektira se u algoritmu te se ponovno prati točka maksimalne snage koja je postignuta približno u 13. sekundi. Statička učinkovitost praćenja točke maksimalne snage za sve razmatrane osunčanosti nije bila manja od 90 %.



a)



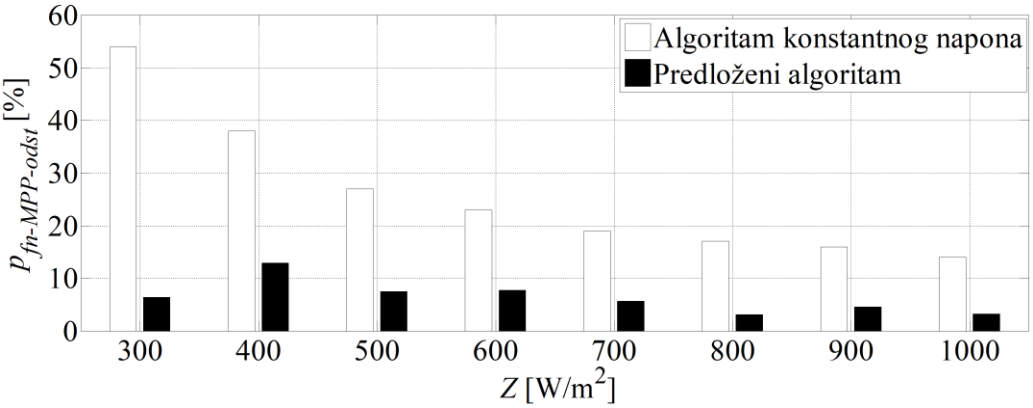
b)

Slika 3.12. Dinamički odzivi snage fotonaponskog izvora (a) i struje fotonaponskog izvora (b) pri skokovitim promjenama osunčanosti [II]

Iz odziva struje i_{fn} prikazanog na slici 3.12b može se primijetiti da postoje razlike u odzivima između razmatranih modela fotonaponskog izvora. Te razlike su posljedica razlike u modeliranju fotonaponskog izvora s obzirom na to da su sve ostale komponente u sustavu iste za sva tri razmatrana modela. Kada se koristi model s promjenjivim kapacitetima predložen u

[I] (model 2 na slici 3.12b), može se uočiti prebačaj u struji i_{fn} za sve tri uvećane prijelazne pojave. Za druga dva razmatrana modela fotonaponskog izvora, prebačaji u struji i_{fn} javljaju se u dvije od tri razmatrane prijelazne pojave.

Statička učinkovitost praćenja točke maksimalne snage algoritma predloženog u [II] uspoređena je s odgovarajućom učinkovitošću postojećeg algoritma konstantnog napona. Ovaj algoritam odabran je za usporedbu s obzirom na to da implementacija oba algoritma zahtijeva mjerenje napona u_{fn}, bez potrebe mjerenja struje i_{fn}. Usporedba je napravljena za model s promjenjivim kapacitetima iz [I], za različite osunčanosti. Slika 3.13 prikazuje rezultate usporedbe postotnih odstupanja od točke maksimalne snage dvaju razmatranih algoritama. Predloženi algoritam značajno je točniji za sve razmatrane osunčanosti. Najveća razlika primijećena je za iznos osunčanosti od 300 W/m^2 i ona iznosi 46 %, a razlika se smanjuje s porastom osunčanosti.

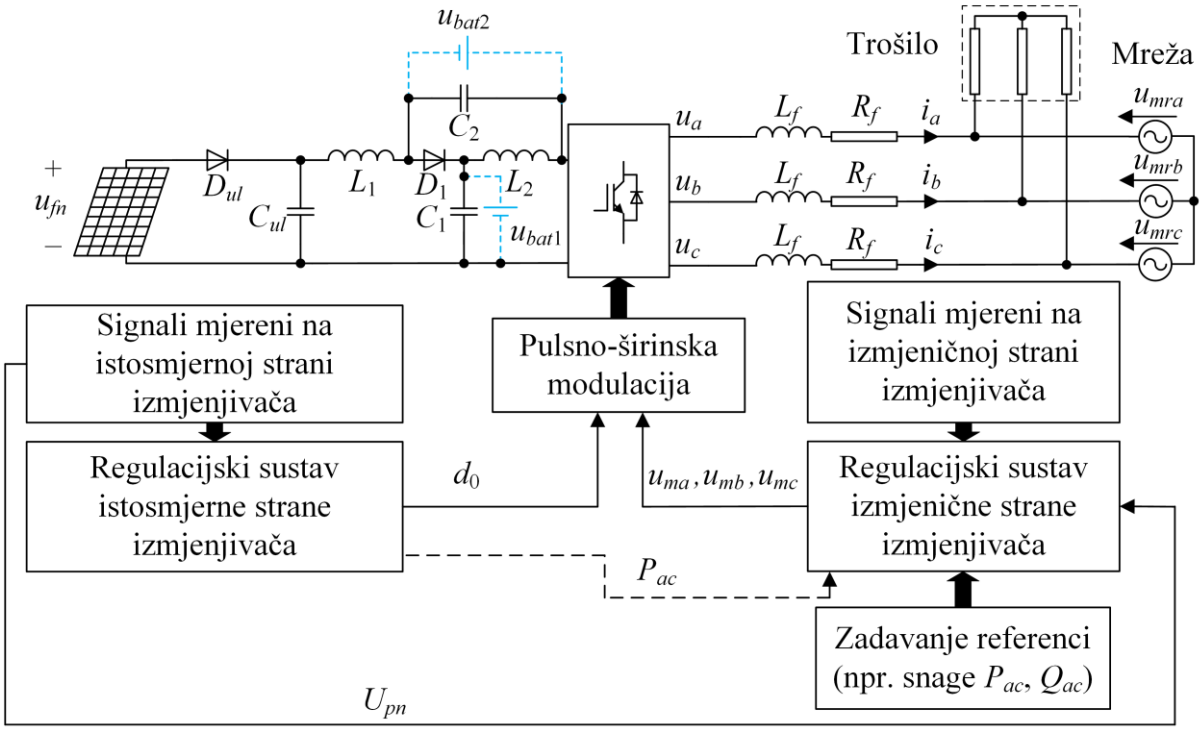


Slika 3.13. Usporedba postotnih odstupanja od točke maksimalne snage između algoritma konstantnog napona i predloženog algoritma [II]

4. REGULACIJSKI SUSTAVI S IZMJENJIVAČEM KVAZI Z-TIPA NAPAJANIM IZ FOTONAPONSKOG IZVORA I BATERIJA

Fotonaponski sustav s izmjenjivačem kvazi Z-tipa moguće je unaprijediti spajanjem baterija odgovarajućeg napona u istosmjerni krug izmjenjivača. Dodavanjem još jednog izvora/spremnika energije u obliku baterija povećava se radno područje sustava. Tako je u sustavu s baterijama koji je spojen na električnu mrežu moguće osigurati kontinuirani rad sustava za vrijeme niskih osunčanosti tako da se manjak energije pokriva iz baterija. Nadalje, dodavanjem baterija u fotonaponski sustav s izmjenjivačem kvazi Z-tipa omogućava se praćenje točke maksimalne snage u otočnom načinu rada, što u sustavu bez baterija nije moguće.

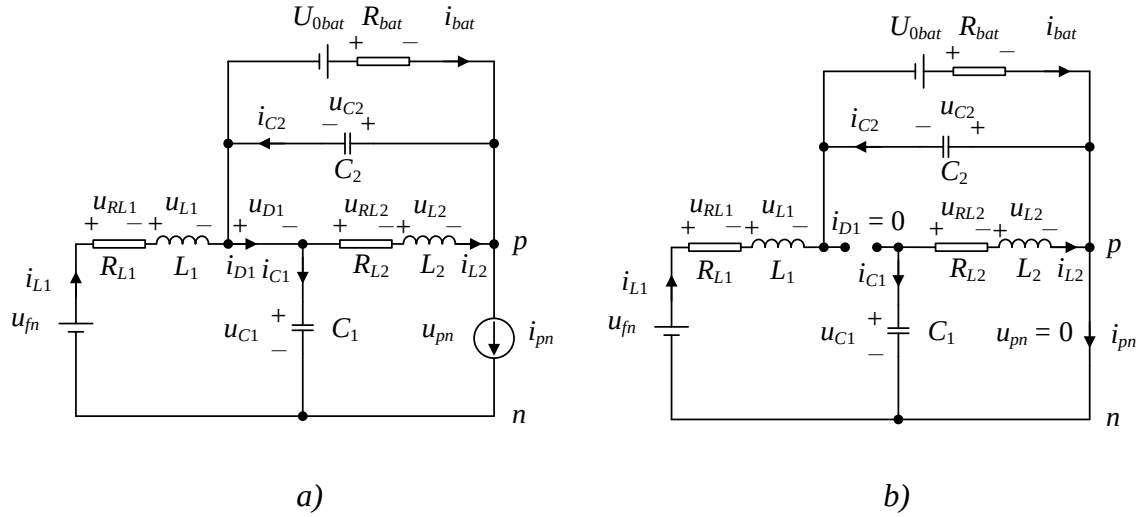
Slika 4.1 prikazuje načelnu shemu regulacijskog sustava s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora i baterija. Baterije se mogu spojiti u istosmjernom krugu paralelno uzdužnom kondenzatoru (C_2) [31, 90-97], [V] ili paralelno poprečnom kondenzatoru (C_1) [98, 99]. Rješenje s baterijama spojenim paralelno uzdužnom kondenzatoru češće je korišteno u literaturi zbog toga što je u tom slučaju zahtijevani nazivni napon baterija manji. Izvedba regulacijskog sustava s izmjenjivačem kvazi Z-tipa i baterijama slična je izvedbi regulacijskog sustava bez baterija. Osnovna razlika je u mogućnosti implementacije regulatora struje baterija. U nastavku je dan matematički model sustava s izmjenjivačem kvazi Z-tipa i baterijama spojenim paralelno uzdužnom kondenzatoru, koji je izveden u [V]. Nakon toga, razmatrani su regulacijski sustavi s izmjenjivačem kvazi Z-tipa i baterijama u otočnom načinu rada i u spoju s električnom mrežom, s naglaskom na sustave predložene u [V].



Slika 4.1. Načelna shema regulacijskog sustava s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora s baterijama spojenim u istosmjernom krugu izmjenjivača [25]

4.1. Matematički model sustava s baterijama

Matematički model izmjenjivača kvazi Z-tipa napajanog iz fotonaponskog izvora s baterijama spojenim paralelno s uzdužnim kondenzatorom (C_2) dobije se na temelju nadomjesnih shema za pojedina stanja izmjenjivača. Nadomjesna shema koja vrijedi tijekom aktivnih i nultih stanja prikazana je na slici 4.2a, a nadomjesna shema koja vrijedi tijekom prostrijelnog stanja prikazana je na slici 4.2b. Tijekom aktivnih stanja izmjenjivač je povezan s mrežom/izmjeničnim trošilom što omogućava tok energije od fotonaponskog izvora i baterija prema mreži/trošilu. U tom slučaju, dioda je propusno polarizirana, naponi na kondenzatorima C_1 i C_2 rastu, dok se struje kroz prigušnice L_1 i L_2 smanjuju. Tijekom prostrijelnog stanja tranzistorski most je u kratkom spoju, a istosmjerna strana je odvojena od mreže/trošila. U tom je slučaju dioda zaporno polarizirana, naponi na kondenzatorima se smanjuju, dok struje kroz prigušnice rastu.



Slika 4.2. Nadomjesna shema izmjenjivača kvazi Z-tipa napajanog iz fotonaponskog izvora s baterijama spojenim paralelno s kondenzatorom C_2 tijekom aktivnih i nultih stanja (a) i prostrijelnog stanja (b)

Usrednjeni matematički model izmjenjivača izvodi se uz pretpostavku simetričnog istosmjernog kruga izmjenjivača, tj. vrijedi da je $L_1 = L_2 = L$, $C_1 = C_2 = C$, $R_{L1} = R_{L2} = R_L$, gdje R_L predstavlja otpor namota prigušnice. Pri tome je zanemaren unutarnji otpor kondenzatora.

Združeni usrednjeni matematički model sustava, detaljno izveden u [V], zapisan u prostoru stanja glasi:

$$F\dot{x} = Ax + Bu \tag{4.1}$$

pri čemu je

$$A = \begin{bmatrix} -R_L & 0 & d_0 - 1 & -d_0 R_{bat} \\ 0 & -R_L & d_0 & (1-d_0)R_{bat} \\ 1-d_0 & -d_0 & 0 & 0 \\ d_0 & d_0 - 1 & 0 & -1 \end{bmatrix},\ B = \begin{bmatrix} 1 & 0 & d_0 \\ 0 & 0 & d_0 - 1 \\ 0 & d_0 - 1 & 0 \\ 0 & 1-d_0 & 0 \end{bmatrix},\ F = \begin{bmatrix} L & 0 & 0 & 0 \\ 0 & L & 0 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & R_{bat}C \end{bmatrix},$$

$$x = \begin{bmatrix} i_{L1} & i_{L2} & u_{C1} & i_{bat} \end{bmatrix}^T,\ u = \begin{bmatrix} u_{fn} & i_{pn} & U_{0bat} \end{bmatrix}^T$$

Varijable stanja u razmatranom sustavu su struje kroz prigušnice (i_{L1}, i_{L2}), napon na kondenzatoru C_1 (u_{C1}) te struja baterija (i_{bat}). Ulazne varijable modela su napon u_{fn}, struja na uzlazu u most izmjenjivača (i_{pn}) i napon otvorenog kruga baterija (U_{0bat}), dok R_{bat} predstavlja unutarnji serijski otpor baterija. Združeni matematički model sustava moguće je linearizirati u području radne točke te dobiti odgovarajuće jednadžbe u Laplaceovom području. Kako bi se dobile tri prijenosne funkcije potrebne za sintezu regulacijskog sustava izmjenjivača kvazi

Z-tipa s baterijama razmatranog u [V], korištena je još jedna jednadžba. To je usrednjena jednadžba koja definira energetsku bilancu idealnog trofaznog mosta izmjenjivača u *dq* koordinatnom sustavu glasi:

$$\frac{3}{2}u_{id}i_d = i_{pn}U_{pn} \tag{4.2}$$

Jednadžbe združenog modela (4.1) skupa s jednadžbom (4.2) linearizirane su i prebačene u Laplaceovo područje. Na temelju jednadžbi u Laplaceovom području dobivene su tri prijenosne funkcije, pri čemu je detaljan izvod dan u [V]. Prijenosna funkcija struje i_{bat} po struji i_d korištena za sintezu regulacijskog sustava u spoju s električnom mrežom dana je kako slijedi [V]:

$$G_{\tilde{i}_d}^{\tilde{i}_{bat}} = \frac{1}{4}\frac{N_3 s^3 + N_2 s^2 + N_1 s + N_0}{K_4 s^4 + K_3 s^3 + K_2 s^2 + K_1 s + K_0} \tag{4.3}$$

pri čemu je

$$N_0 = 3M_a R_L + 3D_0 M_a R_{fn},\ N_1 = 3M_a L + 3CM_a R_L^2 + 3CM_a R_{fn} R_L,\ N_2 = 6CM_a L R_L + 3CM_a R_{fn} L,$$

$$N_3 = 3CM_a L^2,\ K_0 = 2D_0^2 R_L + 4D_0^2 R_{bat} + D_0^2 R_{fn} - 2D_0 R_L - 4D_0 R_{bat} + R_L + R_{bat},$$

$$K_1 = L - 2D_0 L + 2D_0^2 L + CR_L^2 + 2CR_L R_{bat} + CR_L R_{fn} + CR_{bat} R_{fn} + 4CD_0^2 R_L R_{bat} + 2CD_0^2 R_{bat} R_{fn} - \\ - 4CD_0 R_L R_{bat} - 2CD_0 R_{bat} R_{fn},$$

$$K_2 = 2CLR_L + 2CLR_{bat} + CLR_{fn} + C^2 R_L^2 R_{bat} - 4CD_0 LR_{bat} + 4CD_0^2 LR_{bat} + C^2 R_L R_{bat} R_{fn},$$

$$K_3 = CL^2 + 2C^2 LR_L R_{bat} + C^2 LR_{bat} R_{fn},\ K_4 = C^2 L^2 R_{bat}.$$

U prijenosnoj funkciji (4.3) varijable u Laplaceovom području označene su simbolom „~“ poviše varijable, *s* predstavlja kompleksnu varijablu Laplaceove transformacije, dok R_{fn} predstavlja nagib pravca linearizirane strujno-naponske karakteristike fotonaponskog izvora [16, 17]. Druga razmatrana prijenosna funkcija, struja i_{bat} po faktoru d_0, definirana je kako slijedi [V]:

$$G_{\tilde{d}_0}^{\tilde{i}_{bat}} = \frac{1}{4}\frac{P_3 s^3 + P_2 s^2 + P_1 s + P_0}{K_4 s^4 + K_3 s^3 + K_2 s^2 + K_1 s + K_0} \tag{4.4}$$

pri čemu je

$$P_0 = -4U_{11} + 8D_0U_{11} - 4I_{11}R_L + 4I_{pn}R_L - 4D_0I_{11}R_{fn} + 4D_0I_{pn}R_{fn},$$

$$P_1 = -4I_{11}L + 4I_{pn}L - 4CR_LU_{11} - 4CR_{fn}U_{11} - 4CI_{11}R_L^2 + 4CI_{pn}R_L^2 + \\ + 8CD_0R_LU_{11} + 4CD_0R_{fn}U_{11} - 4CI_{11}R_LR_{fn} + 4CI_{pn}R_LR_{fn},$$

$$P_2 = -4CLU_{11} + 8CD_0LU_{11} - 8CI_{11}LR_L - 4CI_{11}LR_{fn} + 8CI_{pn}LR_L + 4CI_{pn}LR_{fn},$$

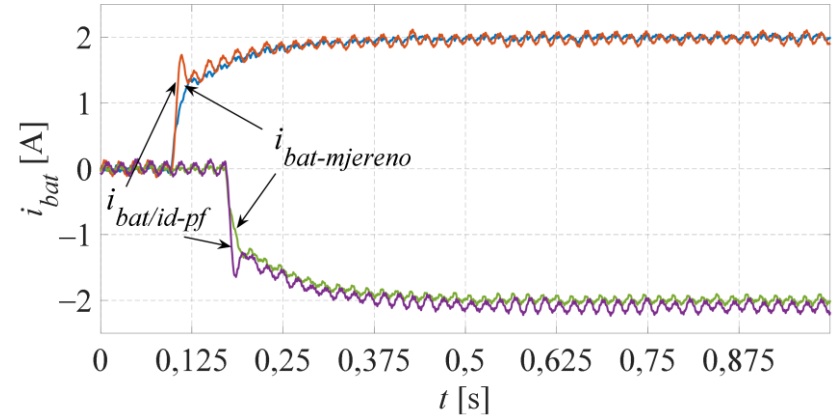
$$P_3 = -4CI_{11}L^2 + 4CI_{pn}L^2.$$

Prijenosne funkcije definirane u (4.3) i (4.4) imaju iste koeficijente u nazivnicima i četvrtog su reda. U prijenosnoj funkciji (4.4) vrijedi $U_{11} = U_{C1} - I_{bat}R_{bat} + U_{0bat}$ te $I_{11} = I_{bat} - 2I_{L1} + I_{pn}$, gdje velika slova u posljednjim jednadžbama predstavljaju srednje vrijednosti veličina. Treba imati na umu da je prijenosna funkcija struje i_{bat} po faktoru d_0 prethodno izvedena u [93-95]. Međutim, u usrednjenom matematičkom modelu korištenom za dobivanje razmatrane prijenosne funkcije uočene su dvije pogreške. Prvo, u sustavu jednadžbi (5) u [94], član $(1 - d_0)U_{0bat}$ u drugoj jednadžbi ima pogrešan predznak, odnosno treba biti zamijenjen članom $(d_0 - 1)U_{0bat}$. Druga pogreška je korištenje jednadžbe za stacionarno stanje za analizu dinamičkog ponašanja sustava. Konačno, treća izvedena prijenosna funkcija, napon u_{fn} po faktoru d_0, korištena za sintezu regulacijske petlje napona u_{fn} dana je kako slijedi [V]:

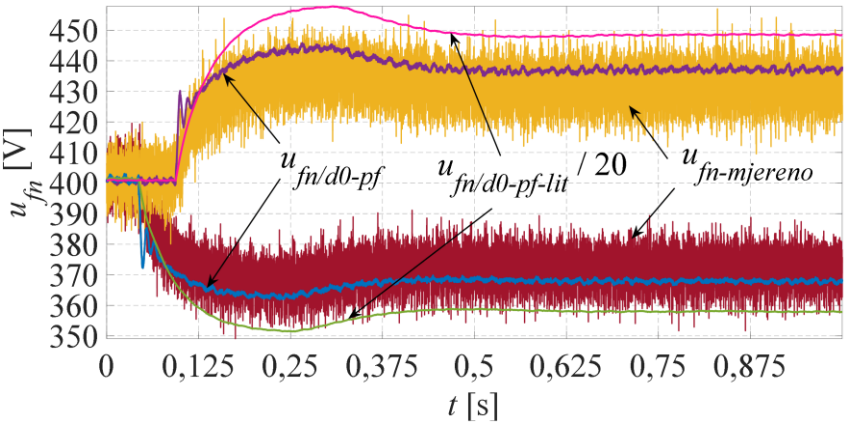
$$G_{\tilde{d}_0}^{\tilde{u}_{fn}} = -R_{fn}G_{\tilde{d}_0}^{\tilde{i}_{L1}} = -R_{fn}\frac{CLU_{11}s^2 + CR_LU_{11}s + U_{11}}{CL^2s^3 + (2CLR_L + CR_{fn}L)s^2 + (L + CR_L^2 + CR_{fn}R_L)s + R_L + D_0R_{fn}} \quad (4.5)$$

Točnost triju prethodno danih prijenosnih funkcija ispitana je u [V] usporedbom valnih oblika signala dobivenih primjenom prijenosnih funkcija i eksperimentalno snimljenih valnih oblika. Rezultati usporedbe odziva dobivenih za skokovite promjene provedene u točkama linearizacije dani su na slici 4.3, dok je ostatak rezultata prikazan u [V]. Slika 4.3a potvrđuje da valni oblik struje i_{bat} dobiven primjenom prijenosne funkcije (4.3) ($i_{bat/id\text{-}pf}$) odgovara valnom obliku mjerene struje ($i_{bat\text{-}mjereno}$) pri skokovitim promjenama struje i_d^* od ± 2 A. Isto vrijedi i za valni oblik napona dobiven primjenom prijenosne funkcije (4.5) ($u_{fn/d0\text{-}pf}$) koji se slaže s mjerenim valnim oblikom $u_{fn\text{-}mjereno}$, što prikazuje slika 4.3b. Odzivi su snimljeni za skokovite promjene faktora d_0 od ± 0,011. Na istoj slici prikazan je i odziv napona u_{fn} dobiven primjenom prijenosne funkcije iz [91] ($u_{fn/d0\text{-}pf\text{-}lit}$). Primjetno je da je taj napon trebalo umanjiti 20 puta kako bi odgovarao mjerenom naponu. Ovako velika pogreška ukazuje na to da u [91] postoji jedna ili više pogrešaka koje je nemoguće otkriti s obzirom na to da usrednjeni matematički model u razmatranom radu nije detaljno izveden. U [91] je navedeno samo da su prijenosne funkcije dobivene uz zanemarivanje članova drugog reda bez preciznijeg

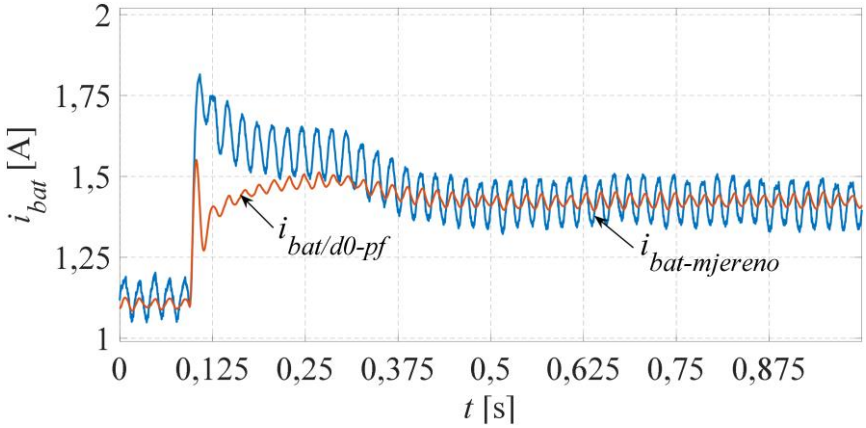
objašnjenja. Slika 4.3c prikazuje odziv struje i_{bat} dobiven primjenom prijenosne funkcije (4.4) ($i_{bat/d0\text{-}pf}$) i mjereni odziv ($i_{bat\text{-}mjereno}$) pri skokovitoj promjeni faktora d_0 od 0,011. Primjećuje se da tu postoje odstupanja tijekom prijelazne pojave, međutim trajanje prijelazne pojave oba signala približno je isto, a i konačne stacionarne vrijednosti se slažu.



a)



b)



c)

Slika 4.3. Eksperimentalno ispitivanje: prijenosne funkcije struje i_{bat} po struji i_d (a), prijenosne funkcije napona u_{fn} po faktoru d_0 (b), prijenosne funkcije struje i_{bat} po faktoru d_0 (c)

Može se zaključiti da je točnost razmatranih prijenosnih funkcija zadovoljavajuća te da se one mogu koristiti za sintezu regulacijskog sustava s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora i baterija.

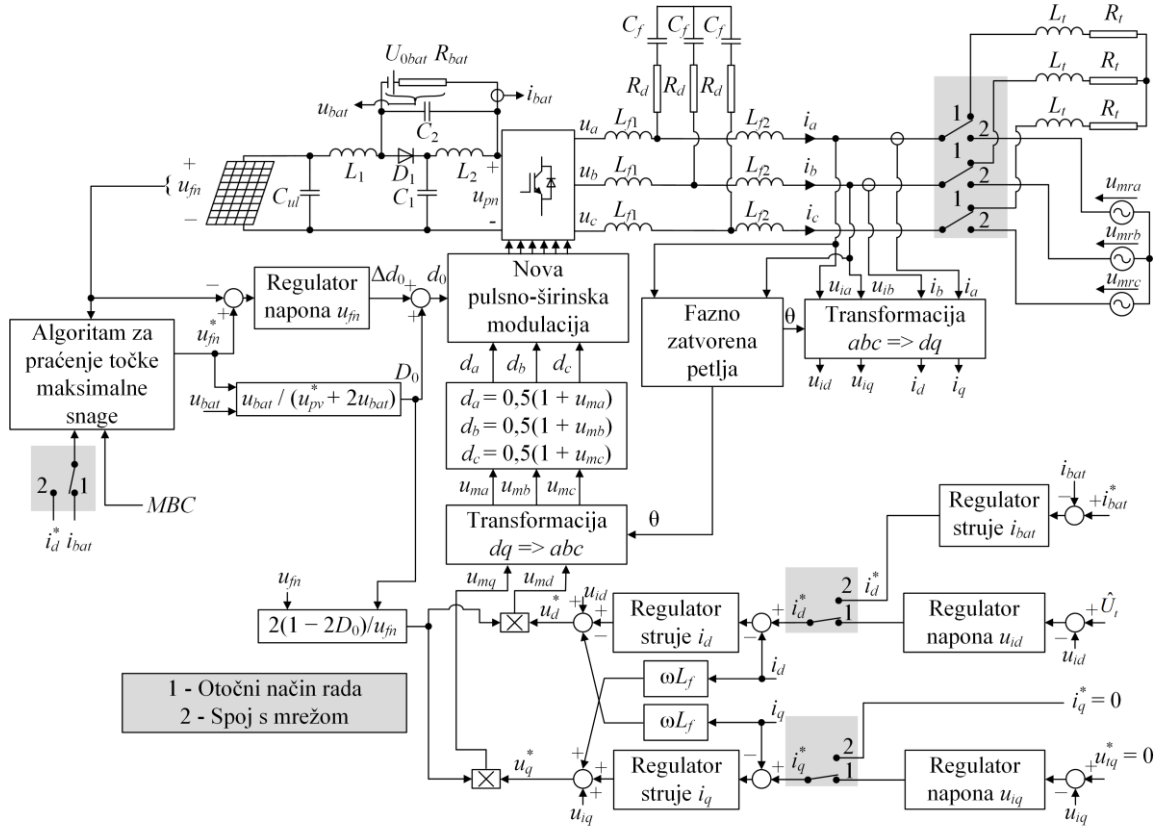
4.2. Regulacijski sustavi s izmjenjivačem kvazi Z-tipa za otočni način rada i za spoj s električnom mrežom

Zadatak regulacijskog sustava u fotonaponskim sustavima s izmjenjivačem kvazi Z-tipa i baterijama spojenim paralelno poprečnom kondenzatoru ovisi o načinu rada. U [93-95, 100], u spoju s električnom mrežom točka maksimalne snage fotonaponskog izvora praćena je promjenom struje i_d, dok je struja i_{bat} regulirana promjenom faktora d_0. Međutim, u [91, 96] u istom načinu rada, napravljeno je suprotno. U otočnom načinu rada točku maksimalne snage moguće je pratiti isključivo promjenom faktora d_0 [90, 92]. Kako bi se osigurala što veća sličnost regulacijskih sustava u otočnom načinu rada i u spoju s mrežom, čime bi se olakšali eventualni prelasci između ova dva načina rada, u spoju s mrežom povoljnije je koristiti pristup iz [91, 96].

Slika 4.4 prikazuje regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora i baterija za otočni način rada i za spoj s električnom mrežom razmatran u [V]. Bitno je naglasiti da prelasci iz jednog načina rada u drugi nisu razmatrani u ovim istraživanjima. Regulacijski sustav izmjenjivača izveden je u *dq* koordinatnom sustavu, pri čemu je izlazni LCL filtar aproksimiran kao L filtar. Ova aproksimacija je opravdana jer je pojas propuštanja frekvencija regulatora mrežnih struja u [V] postavljen u područje u kojem se LCL filtar može aproksimirati s L filtrom uz zadovoljavajuću točnost [101]. Za upravljanje izmjenjivačem korištena je nova pulsno-širinska modulacija s implementiranim mrtvim vremenom kod koje je početak prostrijelnog stanja sinkroniziran s početkom nultog sklopnog stanja [IV].

U spoju izmjenjivača s mrežom, fazno zatvorena petlja sinkronizira vektor izlaznog napona izmjenjivača s vektorom mrežnog napona osiguravajući $u_{id} = \hat{U}_m$, $u_{iq} = 0$. U ovom načinu rada, kružna frekvencija ω jednaka je kružnoj frekvenciji mreže ω_g, pri čemu se kut θ neophodan za transformacije između koordinatnih sustava *abc* i *dq* dobije kao integral kružne frekvencije. Time je osigurano da se promjenom struje i_d^* regulira radna snaga koja se injektira u mrežu, dok se struja i_q^* postavlja u nulu kako bi se spriječilo injektiranje jalove snage u mrežu. U razmatranom sustavu, struja i_d^* dobije se na izlazu regulatora struje baterija, čiji su

parametri dobiveni u [V] sintezom odgovarajuće regulacijske petlje struje baterija. U tu svrhu korištenja je prijenosna funkcija (4.3).



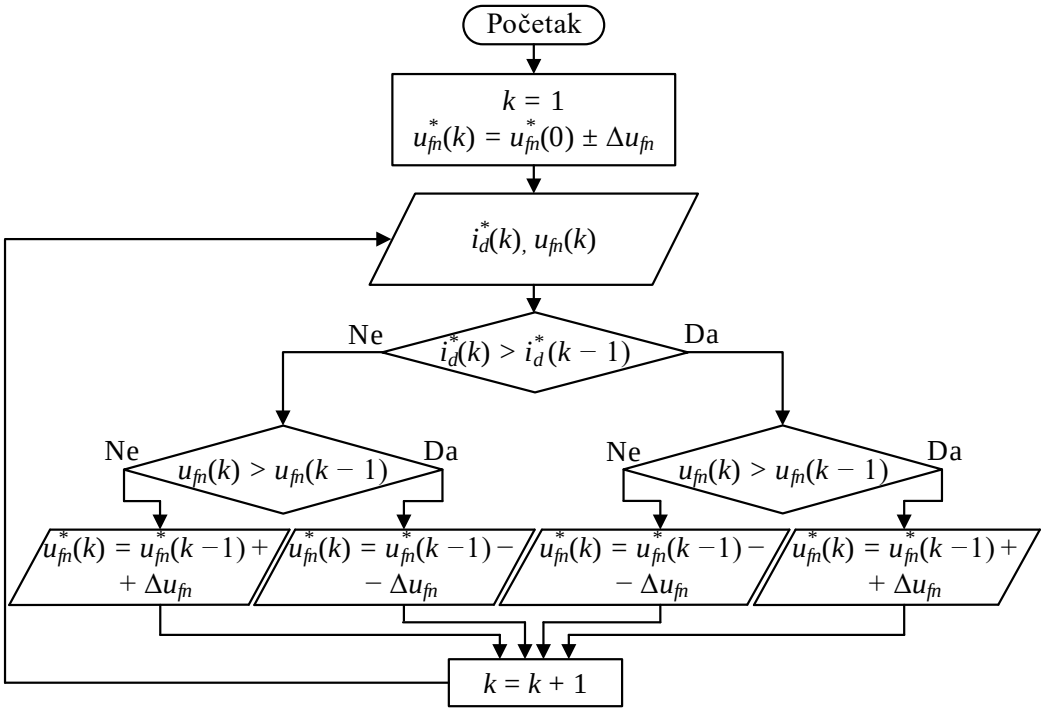
Slika 4.4. Regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora s baterijama za otočni način rada i za spoj s električnom mrežom [V]

U otočnom načinu rada umjesto regulatora struje baterija koriste se regulatori *d* (u_{id}) i *q* (u_{iq}) komponente napona. Referentni napon u_{id}^* jednak je amplitudi osnovnog harmonika zadanog napona trošila $\hat{U}_t$, dok je referentni napon u_{iq}^* postavljen u nulu. Kružna frekvencija u ovom načinu rada jednaka je $2\pi f_l$, gdje f_l predstavlja zadanu frekvenciju osnovnog harmonika napona na trošilu.

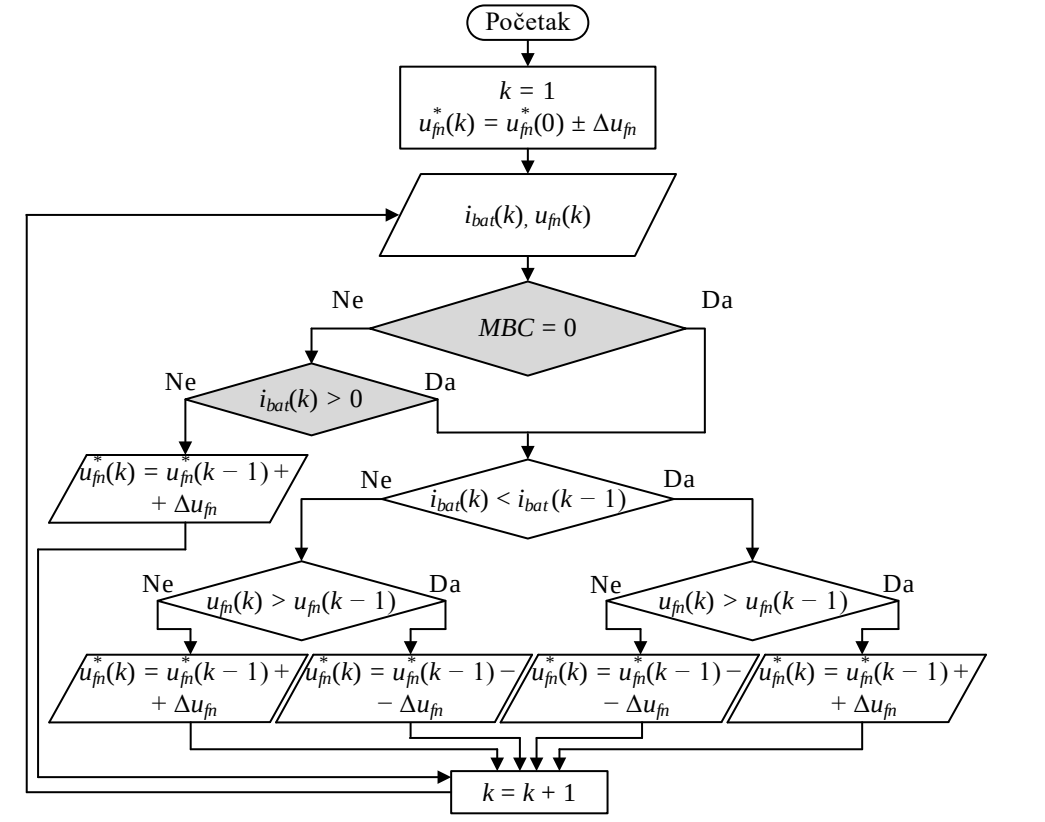
U oba razmatrana načina rada točka maksimalne snage fotonaponskog izvora prati se promjenom faktora d_0. To je omogućeno dodavanjem baterija paralelno kondenzatoru C_2. Uzme li se da je napon baterija približno konstantan, prema izrazu (1.5), s promjenom faktora d_0 mijenja se i napon u_{fn}. Ukupni iznos faktora d_0 određen je kao suma faktora dobivenog na izlazu regulatora i odgovarajućeg faktora unaprijedne regulacije D_0 određenog prema izrazu (1.5) kao $U_{bat}/(U_{fn}^* + 2U_{bat})$. Parametri regulatora napona u_{fn} dobiveni su u [V] sintezom regulacijske petlje napona u_{fn}, pri čemu je korištena prijenosna funkcija (4.5). Referencu napona u_{fn}^* daje algoritam za praćenje točke maksimalne snage.

Algoritam predložen u [V] osigurava praćenje točke maksimalne snage fotonaponskog izvora korištenjem unaprijeđenog algoritma pomaka i promatranja. Konvencionalna izvedba ovog algoritma omogućava praćenje točke maksimalne snage na temelju poznavanja trenutnih vrijednosti napona i snage fotonaponskog izvora, što zahtijeva mjerenje struje i napona izvora. Unaprijeđeni algoritam predložen u [V] zahtijeva poznavanje iznosa napona u_{fn} i struje i_d^* u spoju s električnom mrežom, dok u otočnom načinu zahtijeva poznavanje napona u_{fn} i struje i_{bat}. Stoga, nije potrebno poznavati iznos struje fotonaponskog izvora. Budući da se struje i_{bat} i i_d^* koriste u regulacijskom sustavu bez obzira na algoritam za praćenje točke maksimalne snage, unaprijeđeni algoritam omogućava korištenje jednog strujnog senzora manje u odnosu na postojeće algoritme. Period izvršavanja algoritma za praćenje točke maksimalne snage određen je na temelju odziva struje i_{bat} pri skokovitim promjenama faktora d_0 koji je dobiven na temelju prijenosne funkcije (4.4). Pokazalo se da ova prijelazna pojava traje najduže te je sukladno tome odabran period izvršavanja algoritma.

Slika 4.5 prikazuje dijagrame toka algoritama za spoj s električnom mrežom i za otočni način rada. Dijagram toka prikazan na slici 4.5a, koji se koristi u spoju s mrežom, odgovara u potpunosti dijagramu toka konvencionalnog algoritma pomaka i promatranja. Jedina razlika je ta što je snaga fotonaponskog izvora korištena u konvencionalnom algoritmu u ovoj izvedbi zamijenjena strujom i_d^*. To je bilo moguće napraviti zbog činjenice da se u ovom načinu rada struja baterija regulira na konstantnom iznosu, što rezultira približno konstantnom snagom baterija. Dalje, uz pretpostavku približno konstantnih gubitaka izmjenjivača, promjena snage fotonaponskog izvora rezultira približno proporcionalnom promjenom snage koja se daje u mrežu. To znači da maksimum snage injektirane u mrežu koincidira s maksimumom snage iz fotonaponskog izvora. Stoga se za praćenje točke maksimalne snage umjesto snage fotonaponskog izvora može razmatrati snaga koja se injektira u mrežu. Snaga koja se injektira u mrežu može se u *dq* koordinatnom sustavu izraziti kao $3/2\hat{U}_m i_d$. Uzme li se da je mrežni napon $\hat{U}_m$ približno konstantan, promjena snage izvodi se promjenom struje i_d. Umjesto mjerene struje i_d u algoritmu se koristi referentna struja i_d^* jer se pretpostavlja da regulirana struja odgovara referentnoj u stacionarnom stanju. Korištenjem struje i_d^* izbjegava se utjecaj valovanja struje i_d na rad algoritma za praćenje točke maksimalne snage.



a)



b)

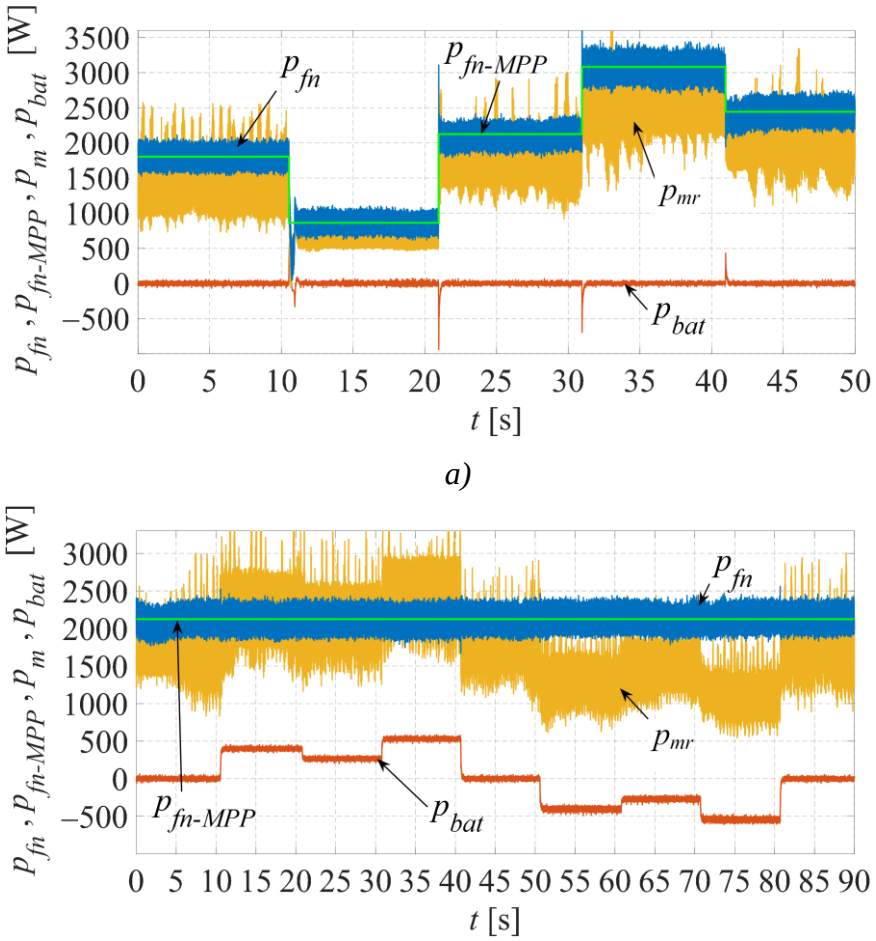
Slika 4.5. Dijagrami toka algoritma za praćenje točke maksimalne snage: u spoju s mrežom (a) i u otočnom načinu rada (b) [V]

Slika 4.5b prikazuje dijagram toka algoritma u otočnom načinu rada, gdje se koristi slična logika kao u spoju s mrežom. U ovom načinu rada može se uzeti da je snaga koja se predaje trošilu sporo promjenjiva u odnosu na period izvođenja algoritma za praćenje točke maksimalne snage pa se s obzirom na algoritam može uzeti da je konstantna. Uz pretpostavku približno konstantnih gubitaka izmjenjivača, promjena snage fotonaponskog izvora rezultira približno proporcionalnom promjenom snage baterija. Povećanje snage iz fotonaponskog izvora dovodi do smanjenja snage iz baterija u načinu pražnjenja baterija, odnosno do porasta snage u načinu punjenja baterija. Uz pretpostavku konstantnog napona baterija, točka maksimalne snage fotonaponskog izvora koincidira s minimalnom strujom iz baterija. Zbog toga se u dijagramu toka na slici 4.5b koristi struja i_{bat} umjesto snage fotonaponskog izvora.

U dijagramu toka prikazanom na slici 4.5b postoje dodatni uvjeti koji su označeni sivom bojom. Tu se javlja signal *MBC* (od engl. *maximum battery charge*), koji definira stanje maksimalne napunjenosti baterija: on iznosi jedan kada su baterije u potpunosti napunjene i ne bi se smjele više puniti, odnosno nula kada je punjenje baterija dopušteno. Kada je punjenje baterija dopušteno, algoritam prati točku maksimalne snage fotonaponskog izvora i baterije se pune ako u sustavu postoji višak snage. S druge strane, ako su baterije u potpunosti napunjene, po potrebi se odstupa od točke maksimalne snage povećavanjem napona u_{fn}, čime se smanjuje snaga fotonaponskog izvora sve dok struja baterija ne postane približno jednaka nuli. Struja baterija može odstupati od nule zbog koraka promjene napona Δu_{fn}, međutim to je zanemarivo odstupanje. Signal *MBC* trebao bi biti izlazna varijabla algoritma koji prati stanje napunjenosti baterija, međutim implementacija tog algoritma nije bila dio istraživanja provedenih u [V].

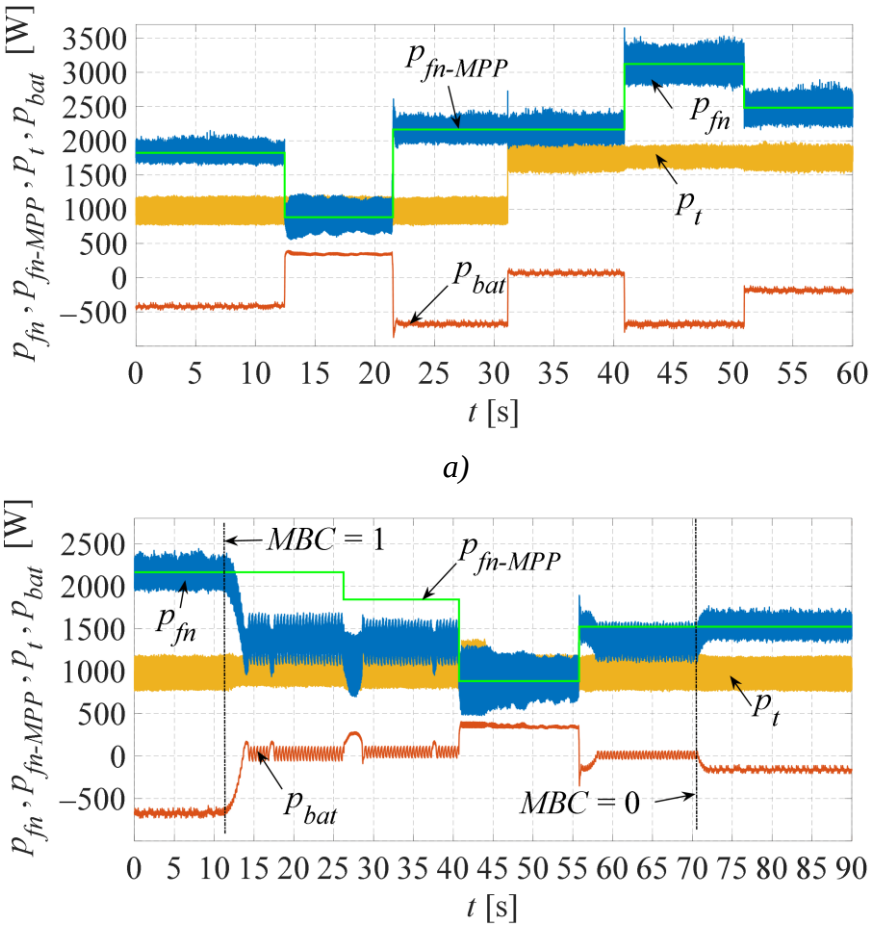
Regulacijski sustav prikazan na slici 4.4 ispitan je eksperimentalno u oba načina rada za raspon osunčanosti od 300 W/m^2 do 1000 W/m^2 i raspon temperatura panela od 10 ˚C do 50 ˚C. U nastavku su prikazani najznačajniji rezultati istraživanja, dok je ostatak rezultata dan u [V]. Slika 4.6a prikazuje snage u sustavu spojenom na mrežu pri skokovitim promjenama osunčanosti i temperaturi panela T = 30 ˚C. Osunčanost je na početku testa iznosila 600 W/m^2 te se mijenjala približno svakih 10 s kako slijedi: 300 W/m^2, 700 W/m^2, 1000 W/m^2, 800 W/m^2. Struja baterija cijelo je vrijeme bila regulirana na 0 A. Na slici 4.6a može se uočiti da je snaga fotonaponskog izvora (p_{fn}) jednaka snazi u točki maksimalne snage ($p_{fn\text{-}MPP}$) za različite iznose osunčanosti. Budući da je i^*_{bat} = 0 A, snaga baterija (p_{bat}) cijelo je vrijeme 0 W, zbog čega se snaga koja se daje u mrežu (p_{mr}) mijenja s promjenom snage p_{fn}. Na slici 4.6b prikazane su snage u sustavu spojenom na mrežu pri skokovitim promjenama struje i^*_{bat}. Na

početku, struja i^*_{bat} bila je postavljena na 0 A te se mijenjala približno svakih 10 s kako slijedi: 1,5 A, 1 A, 2 A, 0 A, –1,5 A, –1 A, –2 A, 0 A. S povećanjem struje i^*_{bat} povećava se snaga koja se injektira u mrežu i obrnuto, dok promjena struje i^*_{bat} praktički ne utječe na snagu p_{fn}, koja je cijelo vrijeme jednaka snazi $p_{fn\text{-}MPP}$.



Slika 4.6. Snage u sustavu spojenom na mrežu pri skokovitim promjenama osunčanosti (a) i skokovitim promjenama reference struje baterija [V]

Slika 4.7a prikazuje snage u otočnom načinu rada razmatranog sustava s izmjenjivačem kvazi Z-tipa za različite iznose osunčanosti i različite iznose otpora simetričnog trofaznog radnog trošila (R_t) spojenog na izlaz izmjenjivača. Napon $\hat{U}_t$ bio je postavljen na iznos $240\sqrt{2}$ V što je približno jednako iznosu napona $\hat{U}_m$ koji je zabilježen u spoju s mrežom. Na početku, osunčanost je bila postavljena na iznos 600 W/m^2 i mijenjala se u 12. sekundi na 300 W/m^2, u 22. sekundi na 700 W/m^2, u 41. sekundi na 1000 W/m^2 te u 51. sekundi na 800 W/m^2. S druge strane, iznos otpora R_t promijenio se skokovito u 32. sekundi sa 175 Ω na 90 Ω.



Slika 4.7. Snage u sustavu u otočnom načinu rada pri skokovitim promjenama osunčanosti i otpora trošila (a) i skokovitim promjenama osunčanosti i signala MBC [V]

I u ovom načinu rada snaga p_{fn} prati maksimalnu snagu $p_{fn\text{-}MPP}$ za različite iznose osunčanosti. Snaga p_{bat} se mijenja jer struja i_{bat} nije regulirana u ovom načinu rada. Skokovita promjena iznosa otpora R_t dovodi do skokovite promjene snage p_{bat}, ali ova promjena nema nikakav utjecaj na snagu p_{fn}. Važno je napomenuti da je u [V] pokazano da sustav radi podjednako dobro ako je na izlaz izmjenjivača kvazi Z-tipa spojeno nelinearno trošilo. Slika 4.7b prikazuje snage u otočnom načinu rada za različite iznose osunčanosti i dvije karakteristične vrijednosti signala *MBC*. Na početku, signal *MBC* je postavljen u nulu, iznos osunčanosti je 700 W/m^2, snage p_{fn} i $p_{fn\text{-}MPP}$ su jednake, a baterija se puni snagom od 600 W. U 11. sekundi signal *MBC* postaje 1, uvećava se napon u_{fn}^* te se postiže snaga p_{bat} približno jednaka nuli čime se sprječava daljnje punjene baterija. Dalje, u 26. sekundi iznos osunčanosti se smanji na 600 W/m^2 te se baterije prazne s malom snagom što je posljedica iznosa koraka promjene napona u_{fn}. Zbog skokovite promjene iznosa osunčanosti na 300 W/m^2 u 41. sekundi snaga p_{bat} postaje pozitivna i baterije se prazne zbog malog iznosa snage p_{pv}. Zbog toga je snaga p_{pv} jednaka snazi $p_{pv\text{-}MPP}$ kako bi se osigurala minimalna struja pražnjenja

baterija. U 56. sekundi dolazi do skokovitog porasta iznosa osunčanosti na 500 W/m^2 koji uzrokuje trenutno povećanje snage p_{fn}, što rezultira negativnom snagom p_{bat}, odnosno punjenjem baterija. Zbog toga se ponovno povećava napon u_{fn}^{*} kako bi se postiglo da snaga p_{bat} bude približno jednaka 0 W. Konačno, u 71. sekundi signal *MBC* postaje 0, čime se dozvoljava punjenje baterija te snaga p_{pv} postaje jednaka snazi $p_{pv\text{-}MPP}$.

5. PREGLED ZNANSTVENOG DOPRINOSA RADOVA

U ovom poglavlju dani su sažetci svih znanstvenih radova na kojima se temelji doktorska disertacija te su posebno istaknuti doprinosi doktoranda u provedenim istraživanjima.

5.1. Novi dinamički model fotonaponskog panela

Sažetak: U ovom radu predstavljen je novi dinamički model fotonaponskog panela. Model panela s dvije diode unaprijeđen je dodavanjem promjenjivog difuzijskog kapaciteta i kapaciteta osiromašenog područja svake od dioda. Eksperimentalno su snimljene strujno-naponske karakteristike monokristalnog fotonaponskog panela za tri različita doba dana. Izmjerene karakteristike uspoređene su s karakteristikama dobivenim pomoću dva najčešće korištena modela: modela s jednom diodom i modela s dvije diode. Predložena nadomjesna shema fotonaponskog panela modelirana je u programskom paketu Matlab Simulink korištenjem osnovnih Simulink blokova. Utjecaj osunčanosti i temperature na iznose kapaciteta te dinamičko ponašanje fotonaponskog panela simulacijski je analizirano.

Doktorandov doprinos

Na početku ovih istraživanja doktorand je napravio usporedbu izmjerenih strujno-naponskih karakteristika fotonaponskog panela s karakteristikama koje su dobivene pomoću dva najčešće korištena modela (modela s jednom diodom i modela s dvije diode). Rezultati usporedbe pokazali su da je model s dvije diode točniji te je doktorand unaprijedio ovaj model dodavanjem promjenjivog difuzijskog kapaciteta i promjenjivog kapaciteta osiromašenog područja obaju dioda. Doktorand je izradio simulacijski model fotonaponskog panela u programskom paketu Matlab Simulink na temelju predložene nadomjesne sheme panela. U nastavku je u simulacijama usporedio novi model s postojećim modelima fotonaponskog panela, a rezultati usporedbe dani su u znanstvenom radu. Doktorand je aktivno sudjelovao u pisanju rada, postupku recenzije te predstavljanju rada na međunarodnoj znanstvenoj konferenciji SpliTech2018.

5.2. Optimizacija proizvodnje električne energije u fotonaponskim sustavima spojenim na izmjeničnu električnu mrežu s izmjenjivačem kvazi Z-tipa

Sažetak: Energija sunčeva zračenja dostupna je praktički u svim dijelovima svijeta i može se pretvarati u električnu energiju unutar fotonaponskih sustava. To dovodi do smanjenja

stakleničkih plinova kao što je ugljikov dioksid. U ovom radu razmatran je izmjenjivač kvazi Z-tipa napajan iz fotonaponskog izvora i spojen na izmjeničnu električnu mrežu. Fotonaponski izvor odabran je tako da se osiguraju odgovarajući iznosi struja i napona koji su zahtijevani na ulazu izmjenjivača kvazi Z-tipa. Novi algoritam za praćenje točke maksimalne snage, predložen u ovom radu, ne zahtijeva mjerenje struje fotonaponskog izvora i ne uzrokuje oscilacije oko točke maksimalne snage za razliku od većine konvencionalnih algoritama. Simulacijski model ovog sustava izrađen je u programskom paketu Matlab Simulink korištenjem isključivo osnovnih Simulink blokova. Simulacijska analiza napravljena je za tri različita modela fotonaponskog izvora kako bi se utvrdio utjecaj dinamike izvora na rad cijelog sustava. Rad sustava ispitan je za širok raspon osunčanosti i temperatura fotonaponskog izvora. Predloženi algoritam za praćenje točke maksimalne snage uspoređen je s konvencionalnim algoritmom konstantnog napona, koji također zahtijeva mjerenje samo napona fotonaponskog izvora. U razmatranom radnom području predloženi algoritam osigurava 453 W više snage iz fotonaponskog izvora (tj. približno 7 % od odgovarajuće nazivne snage).

Doktorandov doprinos

Doktorand je osmislio i izradio novi regulacijski sustav s izmjenjivačem kvazi Z-tipa spojenim na izmjeničnu električnu mrežu. Pri tome je izmjenjivač napajan iz fotonaponskog izvora. Glavni dio predloženog regulacijskog sustava je novi algoritam za praćenje točke maksimalne snage bez oscilacija i bez mjerenja struje fotonaponskog izvora. Doktorand je izradio simulacijski model u programskom paketu Matlab Simulink korištenjem osnovnih Simulink blokova. Model izmjenjivača kvazi Z-tipa preuzet je iz literature, a doktorand je koristio različite modele fotonaponskog izvora kako bi pokazao utjecaj dinamike izvora na rad sustava. Doktorand je napravio simulacijska ispitivanja sustava za široki raspon osunčanosti i temperature te je napravio usporedbu predloženog algoritma za praćenje točke maksimalne snage s postojećim algoritmom konstantnog napona. Također je aktivno sudjelovao u pisanju rada te je bio autor zadužen za korespondenciju s uredništvom časopisa.

5.3. Izračun poluvodičkih gubitaka trofaznog izmjenjivača kvazi Z-tipa

Sažetak: U ovom radu predstavljena su dva nova algoritma za izračun poluvodičkih gubitaka izmjenjivača kvazi Z-tipa. Gubici vođenja i sklopni gubici računati su na temelju strujno-naponskih karakteristika i sklopnih karakteristika koje su dostupne u kataloškim podacima proizvođača poluvodiča. Razmatran je otočni način rada s izmjenjivačem kvazi

Z-tipa, pri čemu je izmjenjivač upravljan sinusnom pulsno-širinskom modulacijom s dodanim trećim harmonikom. Predloženi algoritmi računaju gubitke tranzistora s izoliranom upravljačkom elektrodom i njihovih poprednih dioda, kao i gubitke diode u istosmjernom krugu izmjenjivača. Prvi razmatrani algoritam zahtijeva poznavanje srednje vrijednosti ulaznog napona, srednje vrijednosti struje kroz prigušnicu u istosmjernom krugu, vršnu vrijednost fazne struje, srednju vrijednost amplitudnog indeksa modulacije, faktor trajanja prostrijelnog stanja i fazni pomak između osnovnog harmonika struje i napona izmjenjivača. Njegova primjena moguća je za topologije srodne topologiji izmjenjivača kvazi Z-tipa upravljane sinusnom pulsno-širinskom modulacijom. Drugi razmatrani algoritam zahtijeva trenutne vrijednosti ulaznog napona izmjenjivača, struje kroz prigušnicu u istosmjernom krugu, struje diode u istosmjernom krugu, fazne struje, faktora trajanja prostrijelnog stanja i upravljačkog signala tranzistora. Ovaj algoritam primjenjiv je za različite topologije izmjenjivača i različite pulsno-širinske modulacije. Poluvodički gubici računati primjenom dvaju predloženih algoritama uspoređeni su s eksperimentalno izmjerenim gubicima. Na temelju ove usporedbe, faktor korekcije za sklopne energije tranzistora je utvrđen te je srednja apsolutna pogreška oba predložena algoritma svedena ispod 12 %.

Doktorandov doprinos

Doktorand je izveo analitičke izraze prvog algoritma za izračun poluvodičkih gubitaka izmjenjivača kvazi Z-tipa. U nastavku istraživanja, doktorand je izradio program za izračun poluvodičkih gubitaka na temelju trenutnih vrijednosti mjerenih signala korištenjem programskog paketa Matlab Simulink. Potom je napravio eksperimentalna mjerenja u kojima je usporedio poluvodičke gubitke izračunate primjenom dvaju razmatranih algoritama s eksperimentalno izmjerenim gubicima. Uvidio je da postoje razlike u rezultatima te je došao do zaključka da je to posljedica razlike sklopnih energija tranzistora koje su dane u kataloškim podacima proizvođača tranzistora i stvarnih sklopnih energija tranzistora. Nakon toga, na temelju eksperimentalnih mjerenja, odredio je faktor korekcije sklopnih energija tranzistora čije je uračunavanje dovelo do povećanja točnosti oba predložena algoritma. Također je aktivno sudjelovao u pisanju rada i postupku recenzije.

5.4. Povećanje korisnosti izmjenjivača kvazi Z-tipa: Nova metoda utiskivanja prostrijelnih stanja s mrtvim vremenom

Sažetak: Izmjenjivač kvazi Z-tipa je izmjenjivač s jednim stupnjem pretvorbe koji omogućava pojačanje ulaznog istosmjernog napona uvođenjem tzv. prostrijelnog stanja. Općenito, korisnost izmjenjivača kvazi Z-tipa značajno ovisi o korištenoj metodi utiskivanja prostrijelnog stanja. U ovom radu predstavljena je nova metoda utiskivanja prostrijelnog stanja, tzv. metoda sinkronizacije s nultim stanjem, u kojoj je početak prostrijelnog stanja sinkroniziran s početkom nultog sklopnog stanja sinusne pulsno-širinske modulacije. Na ovaj način, u usporedbi s konvencionalnom metodom utiskivanja prostrijelnog stanja, broj sklapanja po tranzistoru je smanjen. Nulta sklopna stanja detektiraju se korištenjem upravljačkih signala sinusne pulsno-širinske modulacije i ILI logičkih vrata. Željeno trajanje prostrijelnog stanja postignuto je korištenjem integriranog kruga LM555CN. Laboratorijska maketa otočnog sustava s trofaznim izmjenjivačem kvazi Z-tipa je izrađena kako bi se predložena metoda utiskivanja prostrijelnog stanja usporedila s konvencionalnom metodom. Usporedba je napravljena za različite vrijednosti sklopne frekvencije, ulaznog napona, faktora trajanja prostrijelnog stanja i snage trošila. Rezultat implementacije metode sinkronizacije s nultim stanjem je povećanje korisnosti izmjenjivača kvazi Z-tipa za 4 %. Dodatno, neželjena prostrijelna stanja, uzrokovana neidealnim sklopnim karakteristikama korištenih tranzistora, uspješno su eliminirana uvođenjem mrtvog vremena optimalnog trajanja, što je rezultiralo dodatnim povećanjem korisnosti izmjenjivača do 12 % u odnosu na konvencionalnu metodu.

Doktorandov doprinos

Doktorand je u ovom istraživanju osmislio i izradio prototip sklopovlja koje je korišteno za realizaciju i nove i konvencionalne metode utiskivanja prostrijelnih stanja kako bi se ove dvije metode eksperimentalno usporedile. Doktorand je napravio eksperimentalna mjerenja u laboratoriju na temelju kojih su dobiveni rezultati koji su prikazani u znanstvenom radu. Tijekom eksperimentalnih ispitivanja uočio je postojanje neželjenog naponskog pojačanja izmjenjivača koje je eliminirano implementacijom mrtvog vremena. Također je aktivno sudjelovao u pisanju rada i postupku recenzije.

5.5. Fotonaponski sustav s izmjenjivačem kvazi Z-tipa i baterijama: unaprijeđena sinteza regulacijskog sustava utemeljena na novom lineariziranom usrednjenom matematičkom modelu

Sažetak: Ovaj rad se bavi fotonaponskim sustavom s izmjenjivačem kvazi Z-tipa i baterijama spojenim paralelno kondenzatoru s nižim naponskim nivoom u istosmjernom krugu izmjenjivača. Sinteza odgovarajućeg regulacijskog sustava temelji se na tri prijenosne funkcije koje su određene primjenom linearizirano usrednjenog matematičkog modela razmatranog sustava. Prijenosna funkcija struje baterija po *d*-komponenti vektora struje mreže određena je po prvi put u ovom radu za razmatrani sustav te je bila korištena za sintezu regulacijske petlje struje baterija u spoju izmjenjivača s mrežom. Prijenosna funkcija napona fotonaponskog izvora po faktoru trajanja prostrijelnog stanja bila je korištena za sintezu regulacijske petlje napona fotonaponskog izvora, neovisno o tome da li je izmjenjivač spojen s mrežom ili radi u otočnom načinu rada. Ovaj napon je reguliran kako bi se osigurala željena proizvodnja električne energije iz fotonaponskog izvora. Za praćenje točke maksimalne snage, korišten je algoritam pomaka i promatranja koji ne zahtijeva mjerenje struje fotonaponskog izvora, nego umjesto toga koristi struju baterija u otočnom načinu rada i referentnu vrijednost *d*-komponente vektora struje mreže. Odgovarajući period izvođenja algoritma određen je na temelju prijenosne funkcije struje baterija po faktoru trajanja prostrijelnog stanja zbog najdužeg vremena smirivanja pri skokovitim promjenama. Unutar predloženog upravljačkog algoritma ugrađena je zaštita baterija od prekomjernog punjenja u otočnom načinu rada. Razmatrani sustav eksperimentalno je ispitan za široki raspon osunčanosti i temperatura fotonaponskog izvora.

Doktorandov doprinos

Doktorand je izradio novi linearizirani usrednjeni matematički model sustava s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora s baterijama spojenim paralelno uzdužnom kondenzatoru. Na temelju jednadžbi linearizirano usrednjenog matematičkog modela doktorand je primjenom programskog paketa Matlab odredio tri prijenosne funkcije koje su potrebne za sintezu regulacijskog sustava. U nastavku, doktorand je napravio sintezu odgovarajućih regulacijskih sustava u otočnom načinu rada i u spoju s električnom mrežom. Proveo je eksperimentalna ispitivanja sustava u oba razmatrana načina rada. Doktorand je aktivno sudjelovao u pisanju rada i postupku recenzije.

6. ZAKLJUČAK

U ovoj doktorskoj disertaciji razvijeni su regulacijski sustavi s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora, s baterijama i bez njih. Za upravljanje izmjenjivačem kvazi Z-tipa korištena je nova pulsno-širinska modulacija te su dana dva nova algoritma za izračun poluvodičkih gubitaka izmjenjivača.

Metoda utiskivanja prostrijelnih stanja predložena u ovoj disertaciji osigurava sinkronizaciju početka prostrijelnog stanja s početkom nultog sklopnog stanja, čime se broj sklapanja tranzistora u mostu izmjenjivača smanji za približno četverostruki iznos indeksa frekvencijske modulacije. U eksperimentalnim istraživanjima se pokazalo da to dovodi do povećanja korisnosti izmjenjivača do 4 % u odnosu na slučaj kada se koristi konvencionalna metoda utiskivanja prostrijelnih stanja. Tijekom eksperimentalnih istraživanja otkriveno je postojanje neželjenog pojačanja ulaznog istosmjernog napona izmjenjivača zbog postojanja neželjenih kratkotrajnih kratkih spojeva u pojedinim granama mosta izmjenjivača tijekom promjena sklopnih stanja. Neželjeno pojačanje eliminirano je implementiranjem mrtvog vremena odgovarajućeg trajanja, čime je korisnost izmjenjivača povećana do 12 % u odnosu na konvencionalnu metodu.

Dva nova algoritma za izračun poluvodičkih gubitaka analizirana su u nastavku. Prvi algoritam računa gubitke uz pretpostavku sinusne fazne struje i zanemareno valovanje struje kroz prigušnicu, dok drugi algoritam računa gubitke na temelju trenutnih vrijednosti mjerenih signala. U eksperimentalnim istraživanjima pokazalo se da je točnost drugog algoritma veća u odnosu na prvi algoritam, ali je s druge strane njegova implementacija kompleksnija i zahtijeva jedan strujni senzor više. Međutim, pokazalo se da postoje pogreške u oba algoritma za koje se pretpostavilo da su posljedica pogreške sklopnih energija tranzistora preuzetih iz kataloških podataka tranzistora. Zbog toga je uveden korekcijski faktor za sklopne energije tranzistora, dobiven eksperimentalno usporedbom s mjerenim poluvodičkim gubicima, što je dovelo do smanjenja pogreške oba algoritma. U ovim istraživanja za upravljanje izmjenjivačem kvazi Z-tipa korištena je nova metoda za utiskivanje prostrijelnih stanja, a korekcijski faktor računat je u slučaju izostavljenog i u slučaju implementiranog mrtvog vremena. Očekivano, pokazalo se da je korekcijski faktor manji za približno 22 % u slučaju kada je implementirano mrtvo vrijeme. To je posljedica činjenice da su u slučaju izostavljanja mrtvog vremena gubici prouzrokovani neželjenim prostrijelnim stanjima u mostu izmjenjivača neopravdano pridijeljeni pogreškama u sklopnim energijama tranzistora.

Najveća apsolutna pogreška korigiranog točnijeg algoritma koji računa gubitke na temelju trenutnih vrijednosti nije veća od 12 %, dok ta pogreška u slučaju korigiranog algoritma koji računa gubitke uz pretpostavku sinusne fazne struje nije veća od 25 %. Srednja apsolutna pogreška oba predložena algoritma manja je od 12 %.

Novi regulacijski sustav s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora i novi dinamički model fotonaponskog izvora predloženi su u nastavku. Predloženi regulacijski sustav osigurava da fotonaponski izvor radi u blizini točke maksimalne snage uz regulirani tok energije iz fotonaponskog izvora u električnu mrežu. Glavna karakteristika ovog regulacijskog sustava je novi algoritam za praćenje točke maksimalne snage promjenom *d*-komponente vektora struje mreže. Ovo praćenje se odvija bez oscilacija oko točke maksimalne snage, pri čemu se osigurava srednja statička učinkovitost od 94,5 %. Prednost ovog algoritma je što njegova implementacija zahtijeva mjerenje samo napona fotonaponskog izvora, u odnosu na većinu konvencionalnih algoritama čija implementacija zahtijeva i mjerenje struje fotonaponskog izvora. Istraživanja provedena na simulacijskom modelu razmatranog sustava pokazala su da je praćenje točke maksimalne snage moguće za široki raspon osunčanosti i temperatura fotonaponskog izvora. Također, pokazalo se da učinkovitost praćenja točke maksimalne snage ovisi o korištenom modelu fotonaponskog izvora. To znači da je važno u simulacijskom modelu sustava koristiti predloženi dinamički model fotonaponskog izvora kako bi se utjecaj dinamike izvora na rad sustava uzeo u obzir. Usporedbom predloženog algoritma za praćenje točke maksimalne snage s konvencionalnim algoritmom konstantnog napona pokazalo se da je statička učinkovitost praćenja točke maksimalne snage veća i do 46 % u slučaju korištenja predloženog algoritma.

Na kraju su predložena dva nova regulacijska sustava, za otočni način rada i spoj s električnom mrežom, s izmjenjivačem kvazi Z-tipa napajanim iz fotonaponskog izvora i baterija. Za sintezu odgovarajućih regulacijskih petlji korištene su nove prijenosne funkcije dobivene na temelju lineariziranog usrednjenog matematičkog modela sustava. Valjanost predloženih prijenosnih funkcija eksperimentalno je potvrđena te se pokazalo da dinamika odziva dobivenih primjenom prijenosnih funkcija odgovara dinamici izmjerenih odziva, pri čemu odstupanje u srednjoj vrijednosti nije veće od 5 %. U oba razmatrana načina rada korišten je novi unaprijeđeni algoritam pomaka i promatranja za praćenje točke maksimalne snage. Ovaj algoritam osigurava praćenje na temelju napona fotonaponskog izvora i struje baterija u otočnom načinu rada odnosno *d*-komponente vektora struje mreže u spoju s mrežom, čime se izbjegava mjerenje struje fotonaponskog izvora, koje se inače zahtijeva u

konvencionalnoj izvedbi ovog algoritma, zadržavajući pri tom istu statičku učinkovitost praćenja točke maksimalne snage koja se kreće u rasponu od 97 % do 100 %.

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PRILOG A

U nastavku je dan znanstveni rad koji je objavljen u časopisu International Journal of Electrical and Computer Engineering Systems (IJECES).

Semiconductor Losses Calculation of a Quasi-Z-Source Inverter with Dead-Time

Original Scientific Paper

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Abstract *– A quasi-Z-source inverter (qZSI) belongs to the group of single-stage boost inverters. The input dc voltage is boosted by utilizing an impedance network and so called shoot-through (ST) states. In pulse-width modulations utilized for the qZSI, the dead-time is commonly omitted. However, unintended ST states inevitably occur as a result of this action, due to the non-ideality of the switching devices, causing the unintended voltage boost of the inverter and an increase in the switching losses. Hence, the implementation of the dead-time is desirable with regard to both the controllability and efficiency of the qZSI. This paper deals with the calculation of semiconductor losses of the three-phase qZSI with implemented dead time. An algorithm available in the literature was utilized for that purpose. The algorithm in question was originally proposed and applied for the qZSI with omitted dead-time, where the occurrence of unintended, undetected ST states combined with the errors in the switching energy characteristics of the insulated gate bipolar transistor (IGBT) provided by a manufacturer led to errors in the obtained results. However, these errors were unjustifiably ascribed solely to the errors in the switching energy characteristics of the IGBT. In this paper, a new, corrected multiplication factor is experimentally determined and applied to the manufacturer-provided IGBT switching energies. The newly-determined multiplication factor is expectedly lower than the one obtained in the case of omitted dead time. The loss-calculation algorithm with the new multiplication factor was experimentally evaluated for different values of the qZSI input voltage, the duty cycle, and the switching frequency.*

Keywords*: dead-time, loss-calculation algorithm, quasi-Z-source inverter, semiconductor losses, switching energies*

NOMENCLATURE

Symbol	Description
C_f	output filter capacitors
C_1, C_2	impedance network capacitors
D_0	shoot-through state duty cycle
D_1	impedance network diode
e_{Dcond}, e_{Drr}	conduction energy and the reverse recovery energy of the free-wheeling diode, respectively
e_{D1cond}, e_{D1rr}	conduction energy and the reverse recovery energy of the impedance network diode, respectively
e_{Tcond}	conduction energy of the transistor
e_{Toff}	turn-off energy of the transistor
e_{Ton}	turn-on energy of the transistor
f_L	frequency of the load voltage
i_{ce}	collector current
i_{D1}	current of the impedance network diode
i_L	current of the impedance network inductor
i_{ph}, I_{ph}	instantaneous value and the RMS value of the phase current, respectively
k_{sw}	multiplication factor
k_T	coefficient representing voltage dependence of transistor switching losses
L_{f1}, L_{f2}	output filter inductors

L_1, L_2	impedance network inductors
m_a	amplitude modulation index
p	non-ST state switching pulses of the transistor
P_{Dcond}	conduction losses of the free-wheeling diode
P_{D1cond}	conduction losses of the impedance network diode
P_{Drr}, P_{D1rr}	reverse recovery losses of the free-wheeling diode and the impedance network diode, respectively
P_{in}	input inverter power
P_L	losses of the impedance network inductors
$P_{measured}$	measured semiconductor losses
P_{out}	output inverter power
P_{Tcond}	transistor conduction losses
P_{Toff}	turn-off losses of the transistor
P_{Ton}	turn-on losses of the transistor
R_{ac}	output load resistance
R_{ce}	forward resistance of the IGBT
R_D, R_{D1}	forward resistance of the free-wheeling diode and the impedance network diode, respectively
R_d	damping resistance
R_g	gate resistance
R_{L1}, R_{L2}	parasitic resistances of the impedance network inductors
ST_{signal}	shoot-through state signal
T_j	junction temperature
T_{sw}	switching period
t_w	energy accumulation time window
T_0	shoot-through state period
V_{ac}	output voltage RMS value
v_{ce}	collector-emitter voltage
$V_{ce,0}$	threshold voltage of the transistor
v_D	voltage across free-wheeling diode
$V_{D,0}$	threshold voltage of the free-wheeling diode
v_{D1}	voltage across impedance network diode
$V_{D1,0}$	threshold voltage of the impedance network diode
v_{in}, V_{in}	Instantaneous value and the mean value of the inverter input voltage, respectively
V_{pn}	peak value of inverter bridge input voltage
V_{ref}	reference voltage
$v_{refA/B/C}$	reference phase voltages
v_{trian}	carrier triangular signal
τ_d	dead-time of the pulse-width modulation

1. INTRODUCTION

The quasi-Z-source inverter (qZSI), proposed in 2008 [1], is a single-stage inverter with boost capability. It represents a modification of an originally proposed Z-source inverter topology, ensuring continuous input current and lower voltage rating of one of the impedance-network capacitors [2]. The impedance network of the qZSI combined with the additional shoot-through (ST) switching state enables boost of the inverter input voltage. During the ST state, the inverter bridge of the qZSI is short circuited, which is forbidden in conventional voltage-source inverters. Therefore, in order to apply conventional pulse-width modulations (PWMs) for the qZSI, the injection of the ST states has to be additionally enabled.

The control of the qZSI is usually achieved by utilizing the sinusoidal PWM (SPWM) or the space-vector PWM (SVPWM), both with the injected ST states. The most common qZSI-compatible SVPWMs, presented in [3], differ by a number of the inverter legs simultaneously utilized for the ST state injection and by a number of the ST state occurrences within a single switching period. The SVPWM with regard to SPWM achieves higher ac voltage at the inverter bridge output for a given input dc voltage. However, this disadvantage of the SPWM may be overcome by injecting 1/6 of the 3rd harmonic component into the respective modulation signals. The qZSI-compatible SPWMs may be divided into two groups. The first comprises SPWMs in which the ST state duty cycle (D_0) is determined by the amplitude modulation index (m_a). The commonly utilized SPWMs in this group are the simple boost control [4], the maximum boost control [4], and the maximum constant boost control [5]. The second group [6-8] comprises SPWMs which allow the D_0 value to vary regardless of the m_a value as long as the D_0 value is lower than the maximum allowed, which is, in turn, defined by the applied m_a value [5]. In [6], the ST state signal is generated based on the comparison of two dc reference signals (positive and negative) with the carrier signal. In this way, the start of the ST state is unsynchronized with the start of the zero-switching PWM state. This results in the additional zero-switching state occurring between the ST state and the preceding active PWM state, which causes additional switching losses. To overcome this problem, a so-called zero-sync SPWM was proposed in [7], where the start of the ST state is synchronized with the start of the zero-switching state. In the same study, an additional unintended voltage boost was noted in the case of the SPWM with omitted dead-time, which is a consequence of the unintended ST states caused by the non-ideality of the utilized transistors. Consequently, it was in [7] proposed to implement the dead-time within the SPWM so as to eliminate the unintended ST states, resulting in the new dead-time zero-sync (DTZS) SPWM.

The power losses of the qZSI consist of the semiconductor losses and passive component losses. The latter include the inductors' losses, which may be determined as in [9, 10], and the capacitors' losses which are generally considered negligible. The calculation of the semiconductor losses represents a challenging task and many methods have been proposed with this regard [11-17]. In [11], the semiconductor losses were calculated based on the measured voltage and current waveforms of the utilized transistors and diodes. This required sensors with high frequency bandwidth due to the fast transients in the current and voltage of the semiconductor devices. On the other hand, in [12-17], the semiconductor losses were calculated based on the characteristics provided by the semiconductor device

manufacturer. In [12], the switching losses were calculated based on the switching energies determined according to the corresponding switching times and the semiconductor device current and voltage. This approach implies linear change of the current and voltage of the semiconductor device during the switching transition. Another possible approach is to utilize the switching energies characteristics [13-17]. These characteristics are defined as a function of the semiconductor current and are typically approximated by utilizing the linear fitting, whereas more accurate approximation is achieved by utilizing the cubic fitting as in [15]. The losses caused by the unintended ST states were not considered in [12-17], but it was observed in [15] that the loss-calculation error increases with the switching frequency, with the transistor switching losses taking up more than 90% of the total semiconductor losses. This was ascribed to the differences between the actual transistor switching energies and those provided by the manufacturer – determined based on the double-pulse test – which may have been caused by the differences between the test circuitry and the utilized laboratory setup, including parasitic capacitance and additional loop resistance/inductance [18]. Consequently, a multiplication factor (k_{sw}) was introduced for the transistor switching energies to minimize the errors between the measured and calculated losses. However, in this way, the losses caused by the unintended ST states were also ascribed to the errors in the switching energy characteristics, resulting in a presumably overestimated value of $k_{sw} = 1.530$.

This paper deals with the calculation of the semiconductor losses of the qZSI with the DTZS SPWM. The loss-calculation algorithm (LCA), originally proposed and denoted LCA2 in [15], is utilized for that purpose. A new experimentally determined k_{sw} value is utilized for the transistor switching energies, following the same procedure as described in [15]. Finally, the semiconductor losses provided by the LCA with the newly-determined k_{sw} are compared with the experimentally obtained values as well as with the values obtained by another, competing algorithm available in the literature.

2. POWER LOSSES OF THE QZSI

The stand-alone qZSI-based control system is shown in Fig. 1. A symmetrical impedance network is considered in this study, i.e. $L_1 = L_2 = L, C_1 = C_2 = C, R_{L1} = R_{L2} = R_L$. The three-phase inverter bridge is composed of six insulated-gate bipolar transistors (IGBTs) with integrated free-wheeling diodes (FWDs). The LCL filter, composed of the inductors (L_{f1}, L_{f2}), capacitors (C_f), and damping resistances (R_d), is connected to the inverter output. The qZSI supplies the three-phase resistive load (R_{ac}), whereas the control system maintains the required RMS value of the fundamental load phase voltage through the adjustment of m_a. The peak value of the inverter bridge input voltage is defined according to the qZSI input voltage (V_{in}) as follows [1]:

$$V_{pn} = \frac{V_{in}}{1-2D_0} = \frac{V_{in}}{1-2\frac{T_0}{T_{sw}}} \quad (1)$$

where T_0 and T_{sw} represent the ST state period and the switching period, respectively, whereas D_0 represents the ST duty cycle.

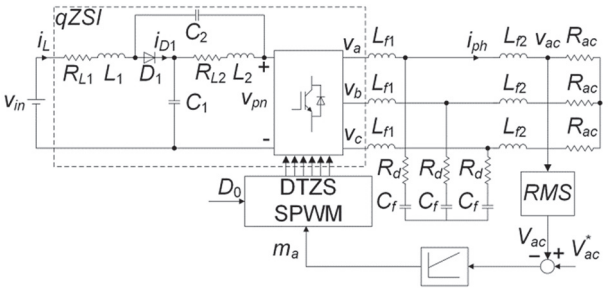

Fig. 1. Stand-alone qZSI-based control system [15]

Fig. 2 shows the waveforms of the reference voltages (v_{refA}, v_{refB}, v_{refC}), the carrier triangular signal (v_{trian}), the ST state signal (ST_{signal}), and the pulses for all the IGBTs (S_{A+}, S_{A-}, S_{B+}, S_{B-}, S_{C+}, S_{C-}) in the case of the DTZS SPWM. The letter in the subscript of "*S*" denotes the corresponding phase, whereas + and – denote the upper and the lower IGBT, respectively. The ST state occurs right at the beginning of each zero-switching state (denoted by the dashed lines). During the ST state, the pulses of all the IGBTs are set to 1. The dead-time (yellow segments) is introduced to postpone the IGBT turn-on pulse ($\tau_d = 0.7$ μs in this study). The considered PWM implied the utilization of the corresponding circuitry, details available in [7].

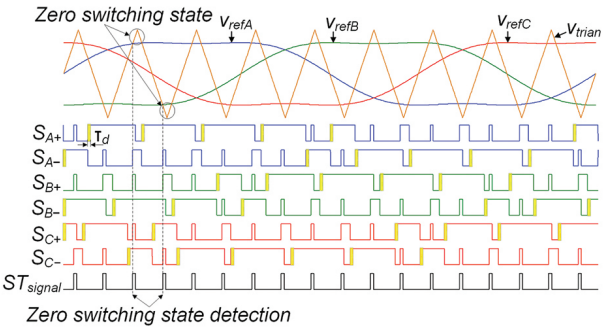

Fig. 2. Waveforms of the dead-time zero-sync SPWM [7]

The power losses of the qZSI represent the difference between the inverter input (P_{in}) and output (P_{out}) powers. These losses include the semiconductor losses and losses of the impedance network inductors and capacitors. The semiconductor power losses are divided into the losses of the IGBTs, the FWDs, and the impedance network diode. As for the IGBTs, the conduction, the switching, and the blocking losses exist, whereas for the diodes the conduction, the reverse recovery, the turn-on, and the reverse losses exist. Generally, the blocking losses of the IGBTs along with the turn-on and reverse losses of the diodes may be considered negligi-

ble. In this study, the semiconductor losses were calculated by utilizing the LCA described in the next section.

3. CALCULATION OF SEMICONDUCTOR LOSSES

The considered LCA was originally applied in [15], where it was denoted LCA2. It enables the calculation of the IGBT and FWD losses in the three-phase inverter bridge and the losses of the impedance network diode. The inverter bridge losses are determined as the losses of a single upper IGBT-FWD pair multiplied by six, based on the assumption of symmetry that holds in the case of the symmetrical output load as is the one utilized in this study. The losses are calculated based on the corresponding energies accumulated in the time window (t_w), as shown in the flow chart in Fig. 3. These energies are obtained from the I–V characteristics and switching energy characteristics of the IGBTs and diodes provided by the semiconductor device manufacturer. The flow chart shown in Fig. 3 may be divided into two parts. The blue-colored part is utilized for the calculation of the IGBT conduction energy accumulated during the ST states and the switching energies of the IGBT and diodes accumulated during the switching transitions between the ST state and the non-ST states. The yellow-colored part of the flow chart shown in Fig. 3 is utilized for the calculation of the energies accumulated during the non-ST states.

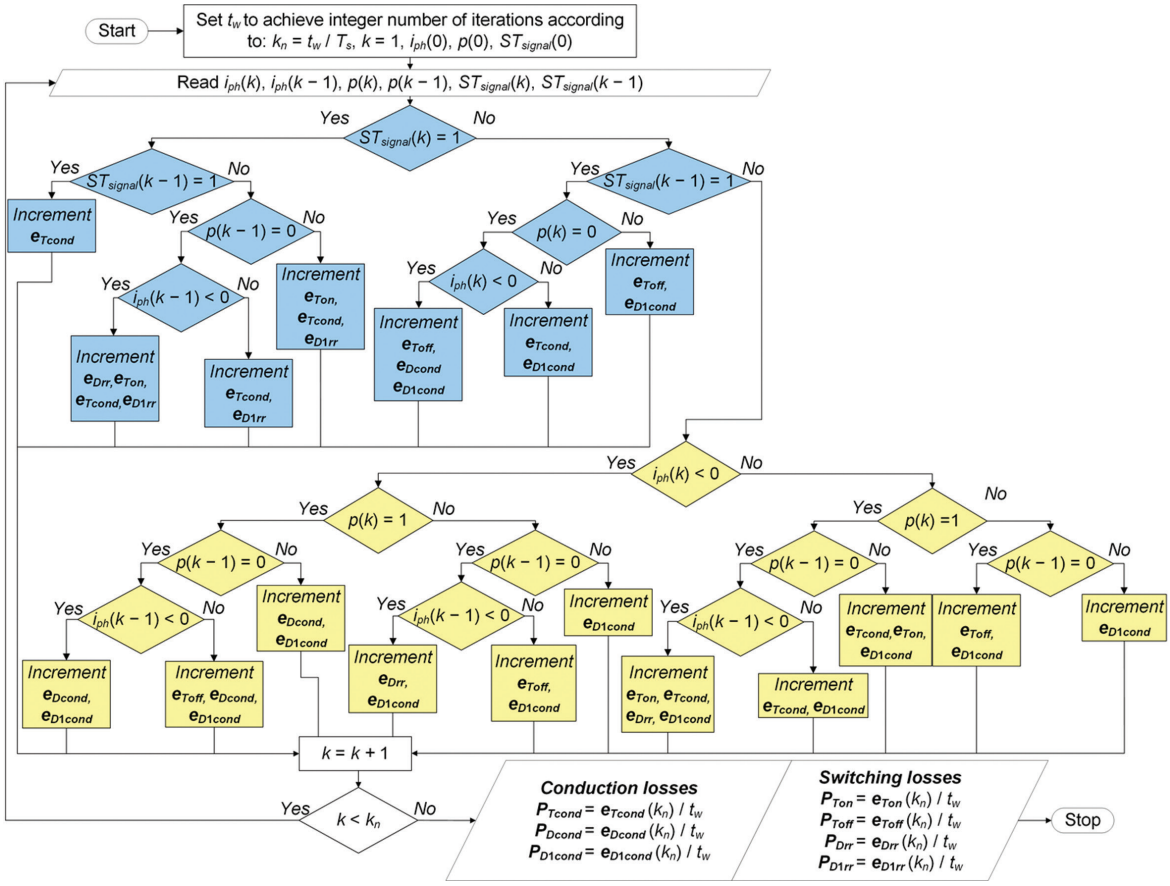

Fig. 3. Flow chart of the LCA [15]

That comprises the conduction and switching energies of the IGBT along with the conduction and reverse recovery energies of the FWD and impedance network diode. The LCA determines which energies should be increased by considering the instantaneous values of the following variables in k^{th} and $(k-1)^{st}$ instants: the non-ST state switching pulses of the IGBT (p), the ST state signal (ST_{signal}), and the phase current (i_{ph}). The IGBT conduction energy (e_{Tcond}) is calculated based on the collector current (i_{ce}) and the collector-emitter voltage (v_{ce}), as follows:

$$e_{Tcond}(k) = e_{Tcond}(k-1) + v_{ce}(k)\left|i_{ce}(k)\right|\left[t(k) - t(k-1)\right]$$
$$v_{ce}(k) = V_{ce,0} + R_{ce}\left|i_{ce}(k)\right| \quad (2)$$

In (2), $V_{ce,0}$ and R_{ce} represent the IGBT threshold voltage and the IGBT forward resistance, respectively (values given in Appendix). During the ST state ($ST_{signal} = 1$), $i_{ce} = 1/2 i_{ph} + 2/3 i_L$, where i_L represents the impedance network inductor current, whereas otherwise $i_{ce} = i_{ph}$.

The conduction energy of the FWD is defined based on the diode forward voltage (v_D) and phase current, as follows:

$$e_{Dcond}(k) = e_{Dcond}(k-1) + v_D(k)\left|i_{ph}(k)\right|\left[t(k) - t(k-1)\right]$$
$$v_D(k) = V_{D,0} + R_D\left|i_{ph}(k)\right| \quad (3)$$

where $V_{D,0}$ and R_D represent the FWD threshold voltage and the FWD forward resistance, respectively (values given in Appendix).

The conduction energy (e_{D1cond}) of the impedance network diode is calculated based on the corresponding threshold voltage ($V_{D1,0}$) and the forward resistance (R_{D1}) (values given in Appendix), as

$$\begin{aligned} e_{D1cond}(k) &= e_{D1cond}(k-1) + \\ &+ v_{D1}(k)\left|i_{D1}(k)\right|\left[t(k)-t(k-1)\right] \\ v_{D1}(k) &= V_{D1,0} + R_{D1}\left|i_{D1}(k)\right| \end{aligned} \quad (4)$$

where v_{D1} and i_{D1} represent the impedance network diode forward voltage and the diode current, respectively.

The IGBT switching losses are calculated based on the corresponding switching energy characteristics. The datasheet of the IGBT-FWD pair utilized in this paper contains the turn-on and turn-off switching energies of the IGBT vs. i_{ce}. These energies are provided for two junction temperatures (T_j = 25 °C and T_j = 150 °C) and for a specific reference value of the inverter bridge input voltage (V_{ref} = 600 V) and the gate resistance (R_g = 10 Ω). Fig. 4 shows the extraction of the characteristics that describe the IGBT turn-on energy (e_{Ton}) vs. i_{ce} by utilizing the cubic fitting. Four coefficients a_0, a_1, a_2, a_3 (values given in Appendix) were obtained by averaging the coefficients obtained for the two provided temperatures. In this study, R_g = 10 Ω was utilized, which corresponds to the value for which the datasheet characteristics were determined.

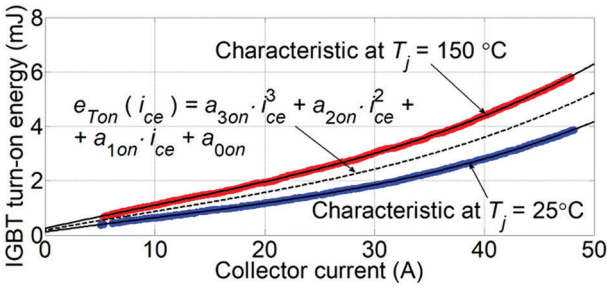

Fig. 4. Turn-on characteristics of the utilized IGBT [15]

The utilized inverter bridge input voltage (V_{pn}) differs from V_{ref} in the datasheet. Therefore, the calculated IGBT turn-on energy was scaled by the ratio $(V_{pn}/V_{ref})^{k_T}$, according to the recommendations in [19], where k_T is the exponent representing the voltage dependance of the IGBT switching losses ranging from 1 to 1.4. Note that the V_{pn} value is determined based on the V_{in} value, as per (1). Finally, by considering all the facts mentioned above, e_{Ton} is obtained as follows:

$$e_{Ton}(i_{ce}) = k_{sw}\left(\frac{V_{pn}}{V_{ref}}\right)^{k_T}\left(a_3 i_{ce}^3 + a_2 i_{ce}^2 + a_1 i_{ce} + a_0\right) \quad (5)$$

In (5), k_{sw} represents a multiplication factor, initially set to 1, introduced to correct the IGBT switching energies, as described in Introduction.

The IGBT turn-off characteristics were extracted in the same way as the turn-on characteristics. The corresponding polynomial is defined as follows:

$$e_{Toff}(i_{ce}) = k_{sw}\left(\frac{V_{pn}}{V_{ref}}\right)^{k_T}\left(b_3 i_{ce}^3 + b_2 i_{ce}^2 + b_1 i_{ce} + b_0\right) \quad (6)$$

where values of b_0, b_1, b_2, b_3 are given in Appendix.

The cumulative values of e_{Ton} and e_{Toff}, obtained based on the flow chart shown in Fig. 3, are calculated as follows:

$$e_{Ton/off}(k) = e_{Ton/off}(k-1) + e_{Ton/off}\left(\left|i_{ce}(k)\right|\right) \quad (7)$$

The reverse recovery energies of the FWD (e_{Drr}) and the impedance network diode (e_{D1rr}) are calculated as follows:

$$e_{Drr}(k) = e_{Drr}(k-1) + e_{Drr}\left(\left|i_{ph}(k)\right|\right) \quad (8)$$

$$e_{D1rr}(k) = e_{D1rr}(k-1) + e_{D1rr}\left(\left|i_{D1}(k)\right|\right) \quad (9)$$

Note that, e_{Drr} and e_{D1rr} utilized in (8) and (9), respectively, are given in Appendix.

4. EXPERIMENTAL INVESTIGATION

Fig. 5 shows the laboratory setup of the stand-alone qZSI-based system. The same measurement equipment and the same sampling procedure as in [15] were utilized for the LCA implementation. Other details about the utilized experimental setup are given in [15].

The measured semiconductor losses ($P_{measured}$) were obtained as $P_{in} - P_{out} - P_L$. The input inverter (P_{in}) power was obtained as the mean value of $v_{in}\cdot i_L$, whereas the output inverter power (P_{out}) was measured by means of the power analyzer Norma 4000 (Fluke). The losses of the inductors (P_L) were calculated as in [9], whereas the losses of the utilized polypropylene capacitors were neglected due to the low ESR value of 7.8 mΩ

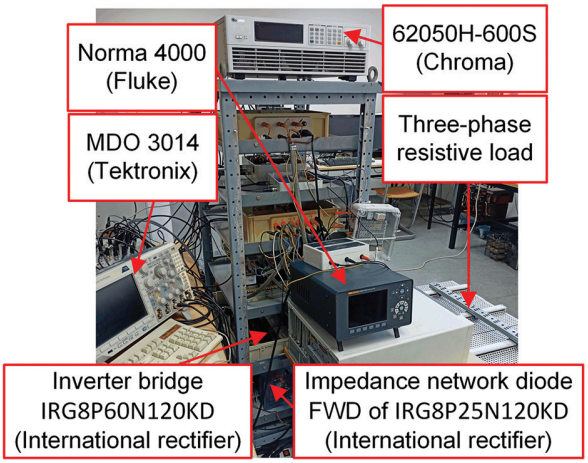

Fig. 5. Laboratory setup of the stand-alone qZSI-based system

4.1 DETERMINATION OF THE MULTIPLICATION FACTOR

The first part of the investigation was carried out to determine the new k_{sw} value applicable for the qZSI

with the DTZS SPWM. For that purpose, the same procedure as in [15] was utilized. The following I_{ph} values were considered: 1.33 A, 1.72 A, 2.12 A, and 2.61 A. During the measurements, f_{sw} and D_0 were set to 5 kHz and 0.22, respectively, whereas V_{in} was set to 450 V, resulting in the constant V_{pn}/V_{ref} ratio with $V_{pn} \approx 800$ V. The reference RMS value (V^*_{ac}) and frequency (f_L) of the fundamental load phase voltage were set to 230 V and 50 Hz, respectively.

The IGBT switching energies were multiplied by k_{sw} to annul the LCA error with respect to $P_{measured}$ for each of the considered I_{ph} values. In this way, the k_{sw} values in the range 1.09 – 1.34 were obtained. The final average value of k_{sw} was calculated as 1.197. As expected, due to the elimination of the unintended ST states and thus the corresponding losses, the new k_{sw} value is about 22% lower than the value previously obtained in [15]. The fact that the new k_{sw} value is still higher than zero speaks in support of the hypothesis that the datasheet values of e_{Ton} and e_{Toff} may differ from the actual ones, as stated in [15]. Note that during the experimental investigation, k_T in (5) and (6) was set to 1.4, which is the highest recommended value [19]. The lower k_T value would result in the higher k_{sw} value.

The comparison between the LCA prior and after the correction of the IGBT switching energies and the measured semiconductor losses is shown in Fig. 6 (left column).

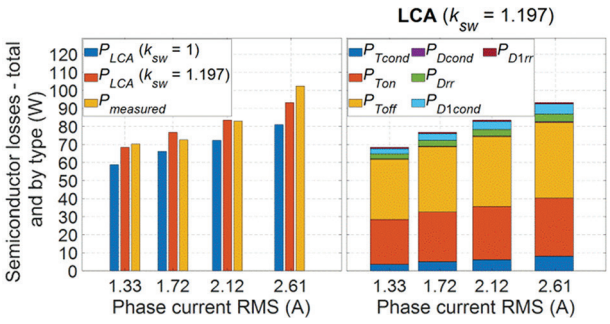

Fig. 6. Measured and calculated semiconductor losses with respect to RMS phase current

In comparison to the results given in [15], the absolute error of the LCA with k_{sw} = 1 (i.e., before the correction) is reduced by approximately 30% solely due to the dead-time implementation. After the application of the corrected factor k_{sw} = 1.197, the highest absolute error was further reduced from 22 W (21%) to 6 W (6%). Note that the error remaining after the correction is probably not related to the conduction losses calculation error, which depends on the chosen LCA sampling period. In this study, the sampling period is set to 2 µs since it has been shown in [15] that the additional reduction of the LCA sampling period does not enhance the LCA's accuracy. The introduced dead-time does not interfere with the LCA's operation because the LCA input variable p represents the actual switching pulses with implemented dead-time.

The right column in Fig. 6 shows the semiconductor losses distribution of the LCA with the applied k_{sw} value of 1.197. The turn-on (P_{Ton}) and turn-off (P_{Toff}) losses of the IGBTs are dominant with the share higher than 90% in the total semiconductor losses. These losses are followed by the conduction losses of the IGBTs (P_{Tcond}) and the conduction losses of the impedance network diode (P_{D1cond}) and FWDs (P_{Dcond}). The reverse recovery losses of FWDs (P_{Drr}) and the impedance network diode (P_{D1rr}) have the lowest share in the total semiconductor losses.

4.2 EXPERIMENTAL EVALUATION OF THE LCA

The second part of the investigation was carried out to evaluate the LCA with the applied k_{sw} in operation ranges that result in different distribution of the semiconductor losses. The semiconductor losses were also calculated by means of another algorithm proposed in [15], where it was denoted LCA1. The corresponding IGBT switching energies were also multiplied by k_{sw} = 1.197.

Fig. 7 shows the corrected calculated and measured semiconductor losses with respect to the switching frequency (f_{sw}), the qZSI input voltage (V_{in}), and the duty cycle (D_0).

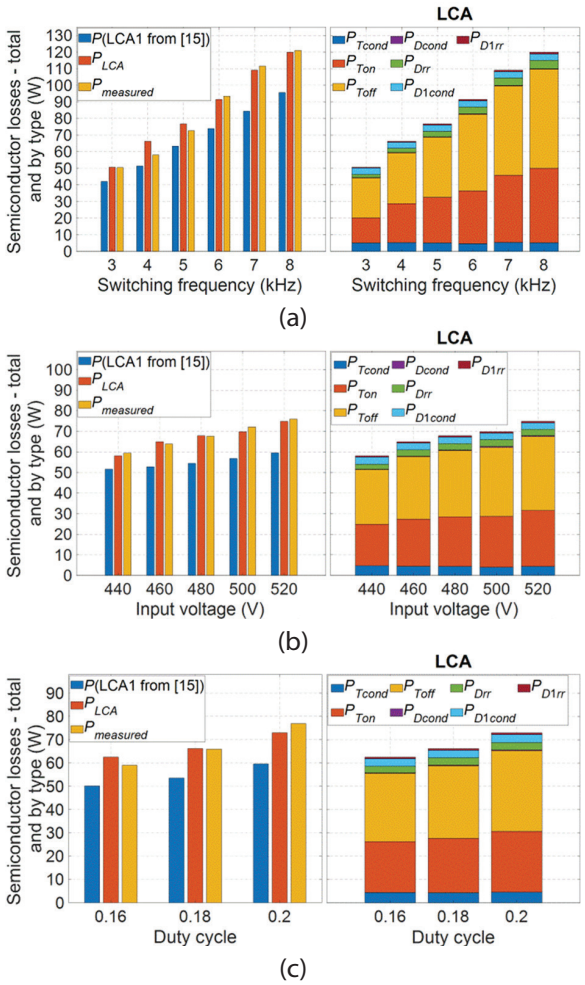

Fig. 7. Corrected calculated (*ksw* = 1.197) and measured semiconductor losses with respect to: switching frequency (a), input voltage (b), and duty cycle (c)

The measurements carried out for this purpose corresponded to the measurements carried out in [15]. The only difference was the utilization of the DTZS SPWM instead of the zero-sync SPWM with omitted dead-time. V_{ac}^{*} and f_L were set to 230 V and 50 Hz, respectively. During the variation of the switching frequency, other parameters were set to the constant values: $D_0 = 0.22$, $I_{ph} = 1.72$ A, $V_{in} = 450$ V. Similarly, the switching frequency was set to 5 kHz when the values of V_{in} and D_0 were varied. The variation of V_{in} was carried out with $D_0 = 0.18$ and $I_{ph} = 1.72$ A, whereas the variation of D_0 was carried out with $I_{ph} = 1.72$ A, $V_{in} = 470$ V. Note that during the variation of V_{in}, the utilization of $D_0 = 0.18$ ensured the highest tolerable V_{pn} value (including transients), which is lower than the maximum allowed value of 1200 V. For the same reason, V_{in} was set to 470 V during the variation of D_0.

The left columns in Fig. 7 indicate that the accuracy of the LCA1 from [15] is lower for all the considered measurement points, with the highest noted error amounting to 25 W (23%), compared to only 9 W (12%) by the LCA. The semiconductor losses distribution of the LCA with the applied $k_{sw} = 1.197$ is shown in Fig. 7 (right columns). This distribution corresponds to the distribution shown in Fig. 6, with dominant P_{Ton} and P_{Toff}.

The second part of the investigation was carried out in order to evaluate the LCA over wide ranges of V_{in} and D_0. The main aim was to consider qZSI applications where V_{in} and V_{pn} vary significantly, such as in the case of a photovoltaic-fed qZSI. In this part of the investigation, the m_a value was set to 0.8, meaning that the output voltage was not controlled, whereas the output load resistance (R_{ac}) was adjusted to maintain 1 kW output power (P_{out}).

Fig. 8 shows the measured and calculated semiconductor losses with respect to V_{in} for the D_0 values of 0.1, 0.15, 0.2, and 0.25.

The results shown in the left columns in Fig. 8 indicate that the semiconductor losses obtained by the LCA (P_{LCA}) closely correspond to the measured losses ($P_{measured}$), with the highest noted error amounting to 11 W (12%). The accuracy of the LCA1 from [15] is lower for all the measurement points, with the highest noted error amounting to 27 W (30%). These results confirm the superior accuracy of the LCA, as previously observed in [15].

The semiconductor losses distribution of the LCA depends on the V_{in} value. In the case of $V_{in} = 200$ V, the conduction losses amount to approximately 60% of the total semiconductor losses for $D_0 = 0.1$. The increase in V_{in} or D_0 causes the increase in V_{pn}, as per (1), and thus the increase in the load voltage due to the constant m_a. Since P_{out} is controlled, higher load voltage implies lower load current and thus lower current through the semiconductors. Therefore, the share of the conduction losses in the total semiconductor losses decreases with the increase in V_{in} or D_0. On the other hand, the share of the switching losses, especially P_{Ton} and P_{Toff}, notably increases with V_{in} and D_0 due to the increase in V_{pn}, as per (1). For example, in the case of applied $V_{in} = 470$ V and $D_0 = 0.25$ the IGBT switching losses amount to 87% of the total semiconductor losses.

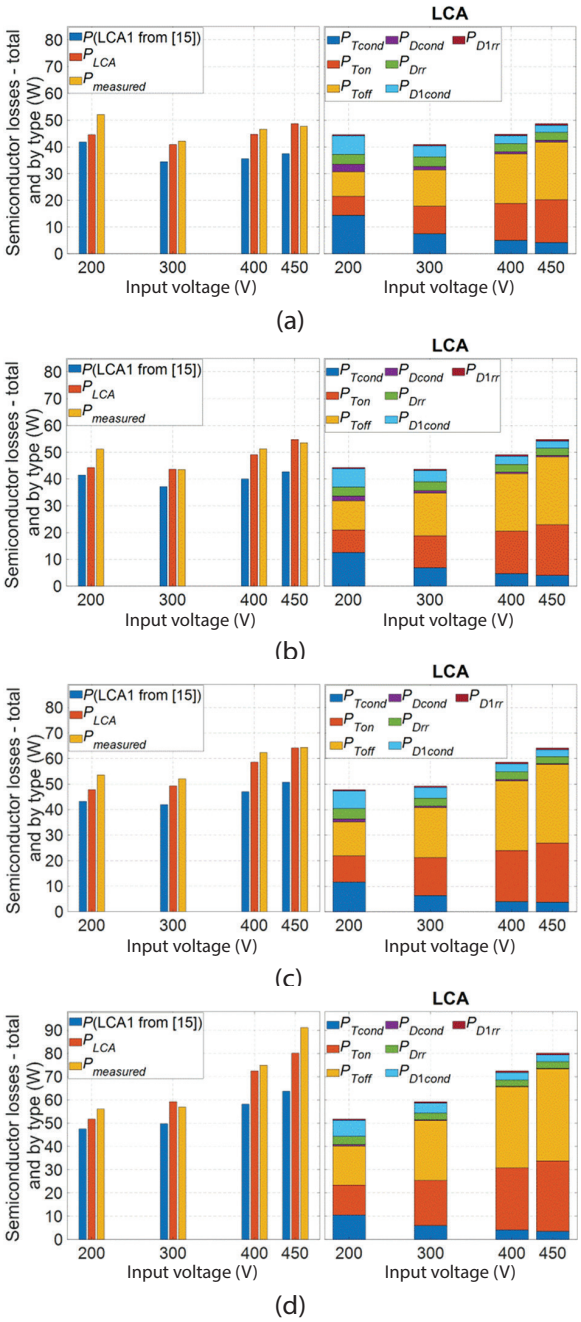

Fig. 8. Corrected calculated ($k_{sw} = 1.197$) and measured semiconductor losses with respect to input voltage for duty cycles of: 0.1 (a), 0.15 (b), 0.2 (c), 0.25 (d)

5. CONCLUSION

In this study, the LCA available in the literature has been successfully applied for the qZSI with the DTZS SPWM. The implementation of the dead-time did not interfere with the LCA's operation, whereas it caused the decrease of the actual inverter losses. As a result, the

corrective multiplication factor for the IGBT switching energies was reduced from 1.530 (omitted dead-time) to 1.197 (implemented dead-time). However, the fact that the new multiplication factor is still different from 1 supports the hypothesis that, in some cases, the manufacturer-provided IGBT switching energies need to be adjusted. Also note that the highest recommended value was utilized for the scaling factor that describes the voltage dependence of the IGBT switching losses. Any reduction of this factor would require higher multiplication factor. Finally, the LCA was experimentally evaluated and compared to another algorithm available in the literature, with the same multiplication factor applied for both the considered algorithms. It turned out that the LCA is overall more accurate with the relative error not exceeding 12%, as opposed to the 30% obtained for the considered competing algorithm.

6. APPENDIX

Parameters and coefficients in (2)-(6)

$R_{ce} = 0.066105\ \Omega$, $V_{ce,0} = 0.6823\ \text{V}$, $R_D = 0.0862\ \Omega$

$V_{D,0} = 0.774\ \text{V}$, $R_{D1} = 0.1225\ \Omega$, $V_{D1,0} = 0.999\ \text{V}$

$a_0 = 0.18$, $a_1 = 0.074$, $a_2 = -7.2 \cdot 10^{-4}$, $a_3 = 2.53 \cdot 10^{-5}$

$b_0 = 0.258$, $b_1 = 0.081$, $b_2 = -1.41 \cdot 10^{-4}$, $b_3 = 0$

Reverse recovery energies in (8), (9)

$$e_{Drr}(i_{ph}) = \left(\frac{V_{pn}}{600}\right)^{0.6} \begin{pmatrix} 9.9 \cdot 10^{-7} i_{ph}^3 - 3.76 \cdot 10^{-4} i_{ph}^2 + \\ + 0.04 i_{ph} + 0.036 \end{pmatrix}$$

$$e_{D1rr}(i_{D1}) = \left(\frac{V_{pn}}{600}\right)^{0.6} \begin{pmatrix} 5.34 \cdot 10^{-6} i_{D1}^3 - 0.0012 i_{D1}^2 + \\ + 0.052 i_{D1} + 0.0145 \end{pmatrix}$$

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PRILOG B

Parametri i koeficijenti u izrazima (2.6)-(2.10)

R_{ce} = 0,066105 Ω, $U_{ce,0}$ = 0,6823 V, R_D = 0,0862 Ω, $U_{D,0}$ = 0,774 V,

R_{D1} = 0,1225 Ω, $U_{D1,0}$ = 0,999 V, k_T = 1,4, k_D = 0,6

a_{0on} = 0,18, a_{1on} = 0,074, a_{2on} = $-7{,}2\cdot10^{-4}$, a_{3on} = $2{,}537\cdot10^{-5}$,

a_{0off} = 0,258, a_{1off} = 0,081, a_{2off} = $-1{,}41\cdot10^{-4}$, a_{3off} = 0,

b_{0D} = 0,036, b_{1D} = 0,04, b_{2D} = $-3{,}76\cdot10^{-4}$, b_{3D} = $9{,}9\cdot10^{-7}$,

b_{0D1} = 0,0145, b_{1D1} = 0,052, b_{2D1} = –0,0012, b_{3D1} = $5{,}34\cdot10^{-6}$

PRILOG C

Tablica C1. Ovisnost iznosa koraka promjene struje i_d^* o iznosu promjene napona u_{fn}

Δu_{fn} [V]	x_2 [A]
– 5	0,025
– 6	0,05
– 8	0,075
– 10	0,1
– 12	0,125
– 14	0,15
– 16	0,2
– 18	0,25
– 20	0,3
– 25	0,35
– 30	0,4
– 40	2

Tablica C2. Ovisnost iznosa faktora d_0 o iznosu napona u_{fn}

Uvjet	d_0
$u_{fn}(k-1) < 515$ V & $u_{fn}(k-1) \geq 515$ V	0,25
$u_{fn}(k-1) > 470$ V & $u_{fn}(k-1) \leq 470$ V	0,3
$u_{fn}(k-1) < 410$ V & $u_{fn}(k-1) \geq 410$ V	0,3
$u_{fn}(k-1) > 360$ V & $u_{fn}(k-1) \leq 360$ V	0,35
$u_{fn}(k-1) < 320$ V & $u_{fn}(k-1) \geq 320$ V	0,35
$u_{fn}(k-1) > 290$ V & $u_{fn}(k-1) \leq 290$ V	0,4

ZNANSTVENI RADOVI NA KOJIMA JE UTEMELJENA DISERTACIJA

Znanstveni rad I

I. Grgić, T. Betti, I. Marasović, D. Vukadinović i M. Bašić, Novel Dynamic Model of a Photovoltaic Module, *2018 3rd International Conference on Smart and Sustainable Technologies (SpliTech)*, 1-6, Split, Hrvatska, 2018.

Novel Dynamic Model of a Photovoltaic Module

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***Abstract*—This paper presents a novel dynamic model of a photovoltaic (PV) module. The two-diode model of a PV module is upgraded with the diodes' parasitic diffusion and junction capacitances, which are, in turn, modeled as variable parameters. The experimental I-V static characteristics were measured for the monocrystalline PV module, at three different stages of a day. The measured characteristics were compared with the commonly used single-diode and two-diode models of the PV module. The simulation model of the proposed PV model was built in the MATLAB-Simulink environment. Influence of the solar irradiation and the temperature on the parasitic capacitances is shown. Also, dynamic behavior of the PV module is analyzed in simulations.**

Keywords—diffusion capacitance; junction capacitance; PV dynamics; PV module; two-diode PV model

I. INTRODUCTION

Photovoltaic (PV) module models are built to describe the PV module behavior in different operating points, which are determined by the solar irradiation level and the PV module temperature. The most commonly used model of the PV module is the single-diode model [1]-[3]. The single-diode PV model presented in [1] consists of a current source, a diode, and series and shunt resistances. In the same paper model parameters estimation method is presented. Similarly, the MATLAB-Simulink model of the single-diode PV model is given in [2]. In [3], effects of changing the solar irradiation level and the temperature are shown. The solar irradiation change affects the short-circuit current, whereas the temperature change affects the open-circuit voltage. The diode saturation current depends on the temperature. However, in [1]-[3], the diode saturation current is calculated form the equations which do not include the PV module voltage and current temperature coefficients.

Another model of the PV module is the two-diode model [4]-[6]. The model presented in [4] consists of a current source and two diodes, but without series and shunt resistances. In the same paper, the algorithm is proposed for finding the diodes' ideality constants a_1 and a_2. MATLAB-Simulink model of the two-diode model which consists of the current source, two diodes, and the series and shunt resistances is given in [5]. The value of the first diode saturation current in [4] and [5] is five to seven times lower than the value of the second diode saturation current. On the other hand, the diodes' saturation currents in [6] are assumed equal. In [6], parameters estimation method is presented, in this method, the series and shunt resistances were changed simultaneously until the maximum power point (MPP) of the PV module is reached. The PV module voltage and current temperature coefficients are included in the equations for the diodes' saturation currents in [4]-[6].

The PV module models considered in [1]-[6] do not account for the PV dynamics. The dynamics of the PV module is modeled by the diodes' parasitic junction and diffusion capacitances. In [7] and [8], one equivalent capacitor is added in the single-diode model. The capacitor value is taken as constant and determined from the experiment. The single-diode model of the PV module is expanded with the variable junction, diffusion and breakdown capacitances in [9]. The effect of the irradiation change, a hot spot and the PV voltage change on the PV module junction, diffusion and breakdown capacitances is shown in [10]. In the same paper, the single-diode model with variable capacitances is given. The single-diode model with the capacitor whose capacitance depends on the PV module current is given in [11]. Determination of the diffusion capacitance and its dependence on the solar irradiation level, the PV module temperature, and the construction material is shown in [12]. However, the model of the PV module is not given and the junction capacitance is neglected. The PV module two-diode model including constant junction and diffusion capacitances is analyzed in [13].

In this paper, a new model of the PV module is proposed. The proposed model consists of a current source, two diodes, series and shunt resistances, and junction and diffusion capacitance of both diodes. For the first time, the two-diode model contains four capacitors, whose values change with respect to the PV module voltage and temperature and the solar irradiation level. The diodes' saturation currents in the proposed model are calculated with the PV module voltage and current temperature coefficients taken into account.

II. PV MODULE MODELS

The PV module static I-V characteristic is not linear. This nonlinearity is usually modeled by means of a current source and a diode, connected in parallel [1]. Two commonly used models are the single-diode model and the two-diode model.

A. Single-diode model of the PV module

The equivalent circuit of the single-diode model of a PV module is shown in Fig. 1. The diode represents the PN

junction, whereas the series and shunt resistances describe the behavior of the PV module at the open-circuit conditions and at the short-circuit conditions, respectively. The solar irradiation current I_{ph} is represented by the current source and is defined as follows [4]:

$$I_{ph} = (I_{sc} + K_i \Delta T)\frac{G}{G_n} \tag{1}$$

where I_{sc} is the short-circuit current, K_i is the current temperature coefficient, G is the solar irradiation level in W/m^2, G_n is the nominal solar irradiation level (usually 1000 W/m^2), ΔT is difference between the module temperature and the nominal module temperature.

The PV module current and the diode thermal voltage are defined as follows [1]:

$$I_{pv} = I_{ph} - I_o\left(e^{\frac{V_{pv}+I_{pv}R_s}{aV_t}} - 1\right) - \frac{V_{pv}+I_{pv}R_s}{R_p} \tag{2}$$

$$V_t = \frac{kT}{q}N_s \tag{3}$$

where I_{pv} is the PV module current, V_{pv} is the PV module voltage, a is the diode ideality constant, V_t is the diode thermal voltage, k is Boltzmann's constant, q is the electron's charge, N_s is the number of series connected cells, and T is the PV module temperature.

The diode saturation current I_0 is defined by the PV module short-circuit current I_{sc}, open-circuit voltage V_{oc}, voltage temperature coefficient K_u, and current temperature coefficient K_i as follows [1]:

$$I_0 = \frac{I_{sc} + K_i \Delta T}{e^{\frac{V_{oc}+K_v\Delta T}{aV_t}} - 1} \tag{4}$$

Most of the parameters needed for the single-diode model are given by PV module manufacturers. Unknown model parameters are the diode ideality constant a, the PV module series resistance R_s, and the PV module shunt resistance R_p.

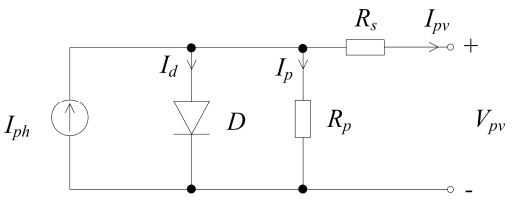

Fig. 1. Equivalent circuit of the single-diode model of the PV module

B. *Two-diode model of the PV module*

The single-diode model of the PV module takes into account diffusion effects, but neglects recombination effects of a diode. In the two-diode model shown in Fig. 2, recombination effects are taken into account by adding a second diode in the model.

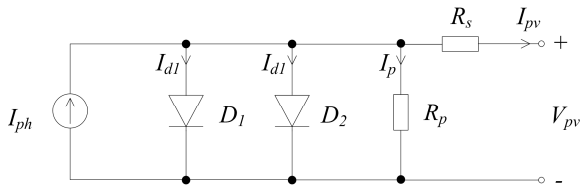

Fig. 2. Equivalent circuit of the two-diode model of the PV module

The PV module current in the two-diode model is [5]

$$I_{pv} = I_{ph} - I_{01}\left(e^{\frac{V_d}{a_1V_t}} - 1\right) - I_{02}\left(e^{\frac{V_d}{a_2V_t}} - 1\right) - \frac{V_d}{R_p} \tag{5}$$
$$V_d = V_{pv} + I_{pv}R_s$$

The diodes' saturation currents are defined as follows [5]:

$$I_{01} = \frac{I_{sc} + K_i\Delta T}{e^{\frac{V_{ocn}+K_v\Delta T}{a_1V_t}} - 1} \tag{6}$$

$$I_{02} = \frac{(T)^{\frac{2}{5}}}{3.77}I_{01} \tag{7}$$

Unknown parameters for this two-diode model are the diodes' ideality constants a_1 and a_2 and the PV module series and shunt resistances R_s and R_p.

III. PV MODULE STATIC CHARACTERISTIC

In this section, the static I-V characteristics obtained by the single-diode and two-diode models were compared with the experimentally obtained static I-V characteristics. The experimental setup is shown in Fig. 3.

Fig. 3. Photography of the experimental measurement configuration

The numbered parts in Fig. 3 are: 1- the monocrystalline PV module SV60-235E produced by Solvis, 2- a PV module temperature sensor, 3- an ambient temperature sensor, 4- EKO MP-170 I-V Checker, 5- a solar irradiation sensor. EKO I-V Checker measures I-V characteristic, the solar irradiation level, the temperature of the PV module, and the ambient temperature. EKO I-V Checker voltage and current measurement accuracy is within ±1% of full scale, whereas temperature measurement accuracy is within ±1.5% of full scale. The experimental results were taken during a sunny day - in the morning, during midday, and in the afternoon.

Fig. 4 shows the experimental I-V characteristics and the mean values of the PV module temperature and the solar irradiation level. For each stage of the day I-V characteristic were recorded five times, repeatedly. The averaged results are shown as dashed lines. The ambient temperatures were 1.5 °C in the morning, 6.26 °C during midday, and 5 °C in the afternoon.

Fig. 5 shows comparison of three averaged experimental I-V characteristic with those obtained by the single-diode and two-diode models. The models' input parameters were taken from the experimental measurements. The characteristics obtained by the single-diode and two-diode models have good fitting with the measured characteristics for all measurements, i.e., the mean absolute error δ is small for both models. The best fitting is achieved for the midday measurements, whereas the poorest fitting is achieved for the afternoon measurements. The two-diode model has lower mean absolute error than the single-diode model for all measurements. Therefore, the two-diode model was further developed to obtain the proposed model, presented in Section IV.

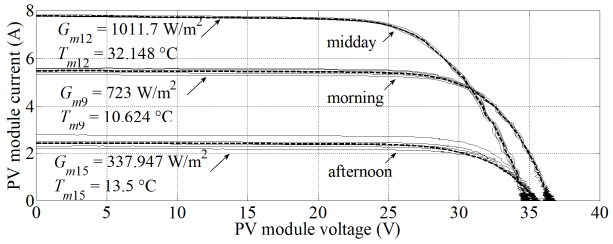

Fig. 4. The PV module experimental static I-V characteristics

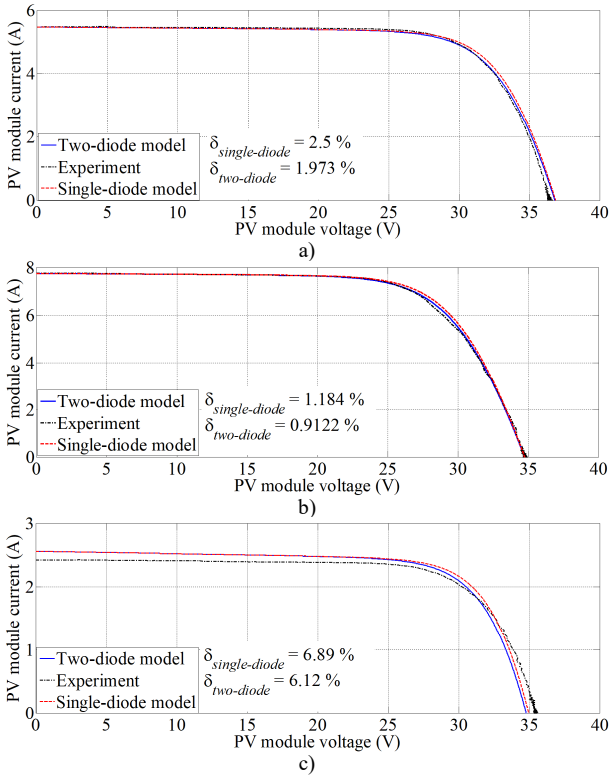

Fig. 5. Simulation and experimental static I-V characteristics: (a) morning measurement, (b) midday measurement, and (c) afternoon measurement

IV. Proposed Model

The equivalent circuit of the proposed model is shown in Fig. 6. Namely, the two-diode model has been expanded in order to include the diodes' parasitic capacitances and thus enable modeling of the dynamic behavior of the PV module.

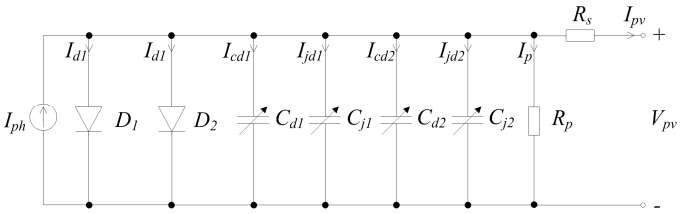

Fig. 6. Equivalent circuit of the proposed model of the PV module

The capacitances C_{j1} and C_{j2} represent the junction capacitance of the diodes D_1 and D_2, respectively. The junction capacitance comes from the charge stored in the depletion region at the semiconductor PN junction. It is dominant in the range of small negative and positive PV module voltages. The junction capacitance can be evaluated as [14]

$$C_j(V_d) = \frac{C_{j0}}{N_s\sqrt{1-\frac{V_d}{N_s\varphi_0}}} \tag{8}$$

where C_{j0} is the zero-voltage capacitance of the PV cell PN junction, φ_0 is the zero-voltage junction potential of the PV cell, V_d is the voltage across diodes (φ_0 is the upper voltage bound for the model, so it should hold that $\varphi_0 > V_{oc}$).

The magnitude of the junction capacitance depends on V_d value. The values of C_{j0} and φ_0 depend on the PV module construction material. They were measured in [9] for the polycrystalline and the monocrystalline Silicon PV cells.

The capacitances C_{d1} and C_{d2} represent the diffusion capacitance of the diodes D_1 and D_2, respectively. The diffusion capacitance comes from the charge stored in the neutral region of the semiconductor, outside the depletion region. It is dominant in the range of high positive voltages, above the maximum power point voltage, where the junction carries significant current. The diffusion capacitance, which is dependent on the PV module temperature and voltage, is given as [9]

$$C_d(T,V_d) = \frac{\tau I_d(T,V_d)}{aV_t(T)} \tag{9}$$

where τ is the mean carrier lifetime.

The PV module current of the proposed model is

$$I_{pv} = I_{ph} - I_{01}\left(e^{\frac{V_d}{a_1V_t}}-1\right) - I_{02}\left(e^{\frac{V_d}{a_2V_t}}-1\right) - \frac{V_d}{R_p} - \frac{d}{dt}\left(q_{j1}+q_{j2}+q_{d1}+q_{d2}\right) \tag{10}$$

The PV module current I_{pv} consists of the static and dynamic parts. The first four terms on the right side of (10), i.e., the current source current, the diodes' currents, and the

shunt resistance current, represent the static part of I_{pv}, whereas the last term on the right side of (10), i.e., the capacitors' currents, represent the dynamic part of the I_{pv}. In the proposed model, all four capacitances are variable. The junction and diffusion capacitor currents are

$$i_{cj} = \frac{dq_j}{dt} = \frac{dV_d C_j}{dt} = \left(C_j + V_d \frac{dC_j}{dV_d} \right) \frac{dV_d}{dt} = C_{jeff} \frac{dV_d}{dt} \quad (11)$$

$$i_{cd} = \frac{dq_d}{dt} = \frac{dV_d C_d}{dt} = \left(C_d + V_d \frac{dC_d}{dV_d} \right) \frac{dV_d}{dt} = C_{deff} \frac{dV_d}{dt} \quad (12)$$

In (11), the effective junction capacitance C_{jeff} is the sum of the static junction capacitance defined in (8) and the dynamic junction capacitance (right term in the bracket). Similarly, the effective diffusion capacitance C_{deff} is defined in (12).

V. Proposed Simulation Model and Results

A. Simulation model

The simulation model of the proposed PV model (Fig. 6) was built in the MATLAB-Simulink using only basic Simulink blocks. The simulation model requires parameters of the PV modules. Some parameters as short-circuit current and open-circuit voltage are given by module manufacturers. However, the values of the series and shunt resistances have to be determined separately. In this paper, these values were determined from the static I-V characteristic: the reciprocal value of the I-V characteristic derivation at open-circuit point (I_{pv}= 0 A) is the value of the series resistance, whereas the reciprocal value of the I-V characteristic derivation at short-circuit point (V_{pv}= 0 V) is the value of the shunt resistance. The PV module used for the experimental measurement does not have a static I-V characteristic in the data sheet and it is, anyway, almost six years old which causes power degradation. Therefore, all the required parameters were determined from the measured I-V characteristic. The standard I-V characteristics are usually given for the PV module temperature T= 25 °C and different values of the solar irradiation. Most PV module manufactures declare the solar irradiation level G= 1000 W/m^2 and the PV module temperature T= 25 °C as default conditions. In this study, during midday experiments the solar irradiation level was G= 1011.7 W/m^2 and the PV module temperature was T= 32.148 °C, which are close to the mentioned default conditions. The values of the parameters for the simulation model were, hence, determined from the midday experiments and are given in Table I. The measured junction and diffusion capacitances parameters C_{j0}, φ_0, and τ for the monocrystalline PV module are taken from [9].

The proposed simulation model is shown in Fig. 7. The capacitances are added into circuit as RC members, to avoid using of the derivation block. However, R_c value is 1 pΩ, so it does not have any significant influence. The PV module capacitances in Fig. 6 were added up and modeled as one equivalent capacitance. This is correct because the capacitors are connected in parallel. The model in Fig. 7 is essentially programmed as a voltage-controlled current source.

TABLE I. Simulation Input Parameters

Parameters	***Values***
Open-circuit voltage, V_{oc}	34.78 V
Short-circuit current, I_{sc}	7.77 A
D_1 ideality constant, a_1	1.4
D_2 ideality constant, a_2	2
Series resistance, R_s	0.35 Ω
Shunt resistance, R_p	250.15 Ω
Number of series connected cells, N_s	60
Voltage temperature coefficient, K_v	-128.7 mV/°C
Current temperature coefficient, K_i	4.355 mA/°C
Midday measurement module temperature, T_{m12}	32.15 °C
Midday measurement irradiation level, G_{m12}	1011.7 W/m^2
Zero-voltage capacitance, C_{j0}	11.7 µF
Zero-voltage junction potential, φ_0	0.82 V
Mean carrier lifetime, τ	5.76 µs

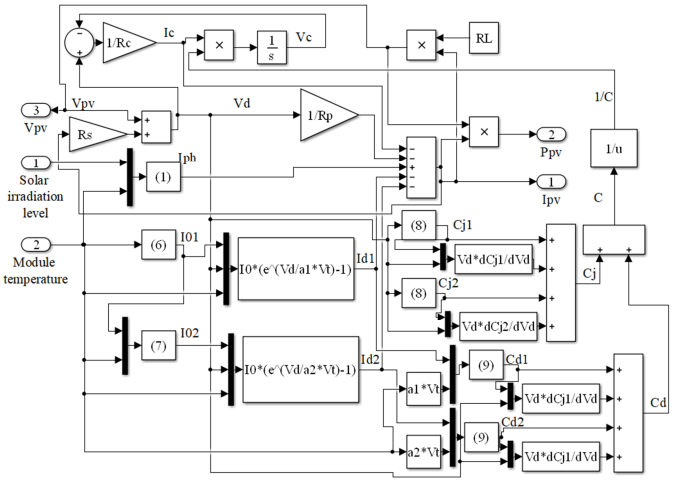

Fig. 7. Proposed PV model in MATLAB-Simulink

B. Simulation results

In most PV module applications, interesting operating point is the MPP. Therefore, in simulations, the MPPs were observed for different operating conditions. The load resistance values at the MPP as a function of the solar irradiation levels were determined. The values of these resistances were calculated from the experimental results for all measurements.

The PV module temperature was different for all measurements (Fig. 4). However, the impact of solar irradiation level on the maximum PV module power is much more pronounced compared to the temperature impact. For example, for the maximum noted temperature change of 22 °C and constant irradiation, the expected variation of maximum power is only 18 W, whereas for the maximum noted irradiation change of 673.76 W/m^2 and constant temperature, the expected variation of maximum power is 140 W.

The R_L-G curve shown in Fig. 8 was obtained by quadratic interpolation:

$$R_{LM} = 1.87 \cdot 10^{-5} G^2 - 0.039G + 24.03 \quad (13)$$

where R_{LM} is the load resistance value at the MPP.

The equivalent junction capacitance is defined as the sum of the D_1 and D_2 junction capacitances. Fig. 9 shows the equivalent junction capacitance as a function of the voltage across diodes, with the MPPs for different solar irradiation levels. The MPPs are shown for 200 W/m^2, 600 W/m^2, and 1000 W/m^2. The same approximation curve is valid for all solar irradiation levels. Variation of the solar irradiation value causes variation of the junction capacitance at the MPP. For example, when G decreases for 800 W/m^2, the equivalent junction capacitance value at the MPP decreases for 0.5 µF.

The equivalent diffusion capacitance is defined as the sum of the D_1 and D_2 diffusion capacitances. The equivalent diffusion capacitance as a function of the voltage across diodes, with the MPPs for different solar irradiation levels, is shown in Fig. 10. Again, as in Fig. 9, the same approximation curve is valid for all solar irradiation levels. The diffusion capacitance value at the MPP also changes when the solar irradiation value changes. For example, when G decreases for 800 W/m^2, the equivalent diffusion capacitance value at the MPP decreases for 18 µF.

In comparison with the equivalent junction capacitance, the equivalent diffusion capacitance decreases much more for the same solar irradiation change. In the MPP area, the equivalent diffusion capacitance value is 20 times greater than the equivalent junction capacitance value. That means that the dynamic behavior of the PV module in the MPP area is mainly determined by the diffusion capacitance.

Another important parameter is the PV module temperature. Fig. 11 shows the equivalent junction capacitance as a function of the voltage across diodes, with the MPPs for different PV module temperatures. The MPPs are shown for the nominal temperature (ΔT = 0 °C), for the temperature variation ±10 °C, and for the temperature variation ±20 °C. When the PV module temperature falls, the equivalent junction capacitance rises and vice versa. This is expected because the junction capacitance depends on V_d. Namely, when the PV module temperature falls, V_d at the MPP rises and that causes the junction capacitance to rise. For ΔT= 40 °C, the junction capacitance value changes for 1 µF.

The equivalent diffusion capacitance as a function of the voltage across diodes, for different ΔT values, is shown in Fig. 12. In this case, different approximation curve is obtained for each ΔT value. The equivalent diffusion capacitance rises when the temperature falls and vice versa. The equivalent diffusion capacitance depends on the diodes' currents, which, in turn, depend on V_d. Namely, when V_d increases, the diodes' currents also increase and that causes the increase of the equivalent diffusion capacitance. For ΔT= 40 °C, the equivalent diffusion capacitance value changes for 12 µF.

The temperature change also affects the equivalent diffusion capacitance more than it affects the equivalent junction capacitance. For the same temperature change, the equivalent diffusion capacitance changes 12 time more than the equivalent junction capacitance.

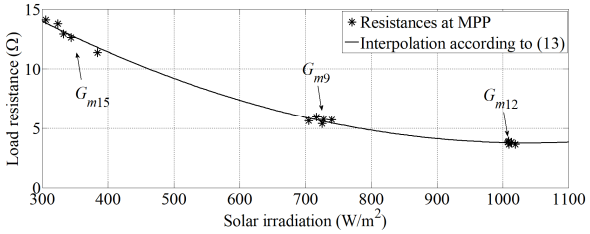

Fig. 8. Load resistance value at MPP vs. solar irradiation

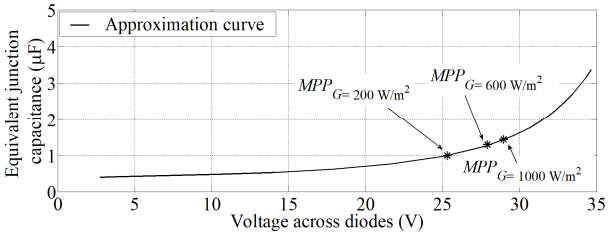

Fig. 9. Equivalent junction capacitance vs. voltage across diodes for different solar irradiation levels and constant nominal temperature

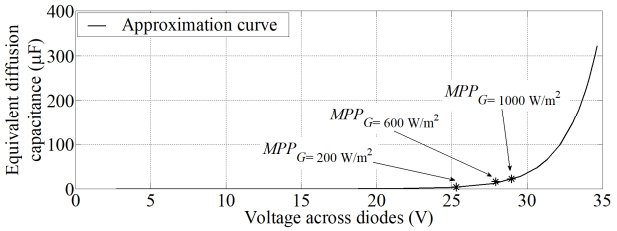

Fig. 10. Equivalent diffusion capacitance vs. voltage across diodes for different solar irradiation levels and constant nominal temperature

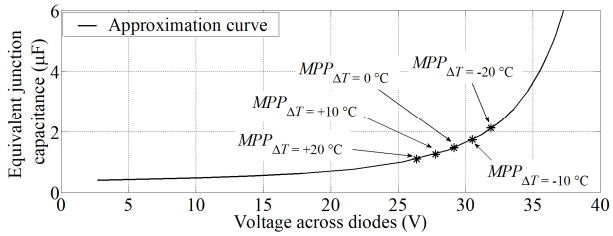

Fig. 11. Equivalent junction capacitance vs. voltage across diodes for different temperatures and constant nominal solar irradiation level

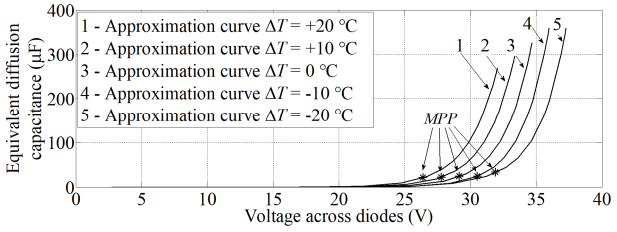

Fig. 12. Equivalent diffusion capacitance vs. voltage across diodes for different temperatures and constant nominal solar irradiation level

Fig. 13 shows the PV module current response to the solar irradiation and load resistance changes. The load resistance was changed so as to achieve the MPP tracking for different operating conditions. The changes in temperature were not considered because these changes are much slower compared to the PV dynamics. The proposed model was compared with

the constant capacitance model whose value at MPP is 5 μF, according to measurement presented in [10].

First, the PV module operates at the MPP. At 120 ms, the solar irradiation changes from 1000 W/m^2 to 300 W/m^2. The PV module after this transition operates in the operating point different from MPP. At 300 ms, the load resistance changes to the value calculated in (13) to achieve the PV module MPP. At 800 ms, the solar irradiation changes from 300 W/m^2 to 800 W/m^2, so the PV module achieves a new operation point, which is not the MPP. At 1500 ms, the load resistance changes to achieve the MPP. In Table II, the PV module current response times are given for the proposed model and the constant capacitance model. For the first change of the solar irradiation level and the load resistance, the response times of the constant capacitance model are about four times longer than the proposed model's response times. For the second change of the solar irradiation level and the load resistance, the proposed model has longer response times than the constant capacitance model, even 12 times during the last solar irradiation change. This is expected because when the solar irradiation level drops, the diffusion and junction capacitance also drop, which causes faster transients, and vice versa.

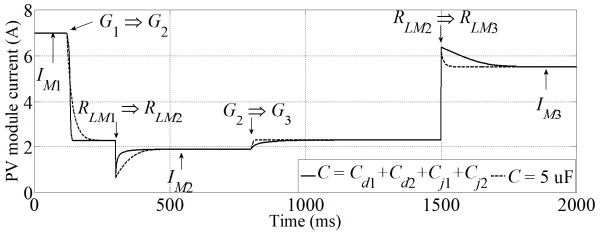

Fig. 13. PV module current response to the solar irradiation and load resistance changes

TABLE II. PROPOSED MODEL AND CONSTANT CAPACITANCE RESPONSE TIMES

Changing parameter	***Changing values***	***Proposed model response time* (ms)**	***Constant capacitance response time* (ms)**
Solar irradiance $G_1 \Rightarrow G_2$	1000 W/m^2 => 300 W/m^2	9.9	44.4
Load resistance $R_{LM1} \Rightarrow R_{LM2}$	3.78 Ω => 14.02 Ω	32.1	91.1
Solar irradiance $G_2 \Rightarrow G_3$	300 W/m^2 => 800 W/m^2	116.4	9.6
Load resistance $R_{LM2} \Rightarrow R_{LM3}$	14.02 Ω => 4.798 Ω	180	21

VI. CONCLUSION

In this paper, a new dynamic model of a PV module is proposed in which variable parasitic junction and diffusion capacitances are introduced. The parasitic capacitances were modeled as variable with respect to the PV module voltage and temperature, and the solar irradiation level.

The comparison of the I-V characteristics obtained with the single-diode and two-diode PV models with the measured I-V characteristics proved that a better curve fitting is achieved with the latter model. Therefore, it was the two-diode model that was further upgraded with the parasitic capacitors.

The simulation results showed the influence of the solar irradiation and temperature influence on the junction and diffusion capacitances. It was also shown that by assuming a constant capacitance value in the PV model, wrong conclusions are obtained about the PV module dynamics. In the future, it is planned to apply the proposed model for development of an MPP tracking algorithm.

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Znanstveni rad II

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Optimization of electricity production in a grid-tied solar power system with a three-phase quasi-Z-source inverter

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ABSTRACT

Solar energy can be harnessed in all areas of the world and directly converted to electricity by means of photovoltaic (PV) systems. This leads to a reduced emission of greenhouse gases such as CO2. In this paper, a grid-tied quasi-Z-source inverter (qZSI) is considered with a PV array connected at the inverter input. The PV array is selected so as to ensure currents and voltages required by the qZSI. A novel maximum power point tracking (MPPT) algorithm, proposed in this study, does not require the measurement of the PV array current and does not oscillate around the maximum power point as opposed to most standard MPPT algorithms. The simulation model of the considered system was built in the MATLAB Simulink environment by using basic Simulink blocks only. The simulation analysis was performed with three PV array models of different complexity to establish the impact of the PV array dynamics on the overall system performance. The operation of the considered system was tested over a wide range of the solar irradiation levels and temperatures of the PV array. The proposed MPPT algorithm is additionally compared with the conventional constant-voltage algorithm, which also requires only measurement of the PV array output voltage. In the considered operating range, the proposed algorithm provides up to 453 W more power from the PV array (i.e., about 7% of the respective nominal power).

1. Introduction

Solar energy represents a clean and fully renewable source of energy. It can be harnessed in all areas of the world and directly converted to electricity by means of photovoltaic (PV) systems. The more electricity is generated by the PV systems, the less of it is required from fossil fuels and, consequently, the emission of greenhouse gases such as CO2 is reduced. In recent years, the share of photovoltaic systems in total electrical energy production is growing rapidly. Since 2000, worldwide installed capacity of the PV systems increased from 2 GW to 400 GW. A PV module converts the solar energy into the electrical energy and represents the clean energy source. Models of the PV module describe its behavior in different operating points, which depend on the solar irradiation level and the PV module temperature. Two most commonly used models of the PV module are the single-diode model (Villalva et al., 2009; Natsheh et al., 2011; Paul et al., 2014) and the two-diode model (Babu and Gurjar, 2014; Gupta et al., 2012; Salam et al., 2010). The single-diode model consists of a current source, a diode, and series and shunt resistances. This model takes into account diffusion effects, but neglects recombination effects of a diode. In the two-diode model recombination effects are taken into account by adding the second diode in the model. In (Grgić et al., 2018) it was shown that the static I-V characteristics obtained by the two-diode model better fits the experimentally obtained I-V characteristic than the one obtained by the single-diode model. In addition, the dynamic behavior of the PV module is modeled by adding the capacitors in the respective model (Suskis and Galkin, 2013; Bisenieks et al., 2008; Kim et al., 2013; Grgić et al., 2018). In (Suskis and Galkin, 2013; Bisenieks et al., 2008), one equivalent capacitor is added to the single-diode model. The capacitor value is taken constant and determined from the experiment. In (Kim et al., 2013) the single-diode model is upgraded with the variable junction, diffusion, and brake down capacitances, whereas in (Grgić et al., 2018) the two-diode model is upgraded with the variable junction and diffusion capacitances. The capacitances in (Kim et al., 2013; Grgić et al., 2018) depend on the voltage across diodes, which, in turn, depends on the solar irradiation level and the PV module temperature.

The electrical power production of the PV module depends on

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0959-6526/

the solar irradiation level and the PV module temperature. For each combination of these two parameters, there is an operating point at which the PV module delivers maximum power. To ensure the PV module operates in the maximum power point (MPP), in various atmospheric conditions, a maximum power point tracking (MPPT) algorithm is used. The MPPT algorithm implementation depends on the PV modules application. There are two large groups of the MPPT algorithms. The first group tracks the MPP based on measurement of the current and the voltage of the PV module (Hohm and Roop, 2003; Babaa et al., 2014; Zainuri et al., 2014; Brambilla et al., 1999; Kazan et al., 2012), whereas the second group of the MPPT algorithms tracks the MPPT based on the model of the PV module and requires the measurement of the solar irradiation level and the PV module temperature (Cristaldi et al., 2013). The second group of algorithms is rarely used due to the fact that the parameters of the PV module are not known accurately, and in fact can vary significantly between the PV modules from the same production run. In addition, the installation of additional sensors increases the cost of the system. The overview of the first group of the MPPT algorithms is given in (Hohm and Roop, 2003; Babaa et al., 2014). In (Hohm and Roop, 2003) the theoretical background of the first group of the MPPT algorithms is given and the operation of the following types of MPPT algorithms is compared: perturb and observe (P&O) algorithm, incremental conductance (IC) algorithm, and constant voltage (CV) algorithm. The comparison proved that the efficiency of the P&O algorithm and the IC algorithm is about 98%, whereas the efficiency of the CV algorithm is about 90%. In (Babaa et al., 2014) the simulation results show that the P&O algorithm exhibits faster dynamic performance and less oscillatory behavior after reaching the steady state than the IC algorithm for wide range of the solar irradiation levels. An MPPT algorithm based on the combination of the P&O and fuzzy logic was proposed in (Zainuri et al., 2014). Simulation and experimental testing has shown that the efficiency of the P&O-fuzzy algorithm is 95%, whereas the efficiency of the classic P&O algorithm is 90%. However, introduction of the fuzzy logic increases the computational complexity, which implies increase of the system costs. In addition, the efficiency of the MPPT algorithm proposed in (Zainuri et al., 2014) depends on the solar irradiation level. For example, the efficiency is 90% for the solar irradiation level 200 W/m^2, whereas the efficiency is 95% for the solar irradiation level 1000 W/m^2. In any case, the model of the PV module used in (Zainuri et al., 2014; Hohm and Roop, 2003; Babaa et al., 2014) does not describe the PV module dynamic behavior. The MPPT algorithms in (Brambilla et al., 1999; Kazan et al., 2012) are developed with respect to the single intrinsic capacitance of the PV module, which represents the PV module dynamic behavior. However, their operation was not tested for multiple connected PV modules.

In many applications of PV systems, connection to the electrical grid is required. Connection of the PV system to the grid can be implemented through the quasi-Z-source inverter (qZSI). In this case, it is necessary to adapt the MPPT algorithm to specific system requirements. In (Park et al., 2009; AsSakka et al., 2017; Li et al., 2010) the grid-tied qZSI with the PV array is described. The MPPT algorithms control the shoot-through (ST) duty ratio (D_0) of the qZSI, whereas the reference d-axis current on the grid side is obtained at output of the proportional integral (PI) controller of the impedance network capacitor voltage. In (Park et al., 2009) the P&O MPPT algorithm was implemented, whereas in (AsSakka et al., 2017) the IC MPPT algorithm was implemented. The two stage control for the standalone qZSI proposed in (Li et al., 2010) is divided into the dc side control and the ac side control. The dc side PI controller controls the impedance network capacitor voltage and outputes the ST duty ratio, whereas the ac side PI controller provides the required voltage on the ac side and defines the sine pulse width modulation (SPWM) signals. In (Sun et al., 2013; Khajesalehi et al., 2015) batteries are additionally introduced in parallel with the lower-voltage capacitor in the impedance network of the qZSI. In (Sun et al., 2013) the P&O MPPT algorithm controls the ST duty ratio of the grid-tied qZSI, whereas the power injected to the grid is determined by the reference d-axis current on the grid side. The batteries cover the difference between the PV array power and the power injected to the grid. In (Khajesalehi et al., 2015) the MPPT algorithm and the control of the batteries current were realized for the standalone and grid-tied qZSI. The MPPT algorithm controls the ST duty ratio, whereas the reference d-axis current on the grid side is the output of the PI controller of the batteries current. The MPPT algorithms proposed in (Park et al., 2009; AsSakka et al., 2017; Li et al., 2010; Sun et al., 2013; Khajesalehi et al., 2015) track the MPP by controlling the ST duty ratio which requires high sampling frequencies (i.e., over 100 kHz). This represents a major requirement for a microprocessor given the real-time execution of the MPPT. In addition, the results demonstrate the system behavior for various solar irradiation levels, but do not demonstrate the system behavior for different PV array temperatures.

This paper considers the grid-tied qZSI in the PV application. The corresponding control system ensures synchronization of the qZSI and the grid, ensures the required power factor, ensures the stable operation, and provides the MPP of the PV array. A novel P&O-based MPPT algorithm is proposed. The input variables of the proposed MPPT algorithm are the PV array voltage and the reference voltages for the SPWM of the qZSI in the *dq* coordinate system. The proposed MPPT algorithm consists of two control stages. In the first control stage the MPP is tracked by controlling the reference d-axis current on the grid side, instead of controlling the ST duty ratio as in (Park et al., 2009; AsSakka et al., 2017; Li et al., 2010; Sun et al., 2013; Khajesalehi et al., 2015), to avoid high sampling frequencies. In the second control stage the duty ratio is changed in predetermined discrete steps and the modulation index transients are alleviated to maintain stable operation the system. The proposed MPPT algorithm was applied for three two-diode models of the PV array. The first is the standard model in which the dynamic behavior of the PV array is neglected (Babu and Gurjar, 2014; Gupta et al., 2012; Salam et al., 2010). In the second model the dynamic behavior of the PV array is modeled by the diodes' diffusion and junction capacitances (Grgić et al., 2018), which are variable, whereas in the third model the dynamic behavior is modeled by a constant capacitance (Grgić et al., 2018). To our best knowledge, this is the first time the dynamic model of the PV array was combined with the qZSI. The simulation model of the considered system was built in the MATLAB Simulink by using basic Simulink blocks only. The simulation results are shown for wide range of the solar irradiation levels and the PV array temperatures. The proposed MPPT algorithm is additionally compared with the conventional CV algorithm reported in (Tofoli et al., 2015), which also requires only measurement of the PV array output voltage.

2. Photovoltaic array modeling

2.1. Model of a photovoltaic module

The equivalent circuit of the standard two-diode model of a PV module is shown in Fig. 1. The diodes represent the PN junction, whereas the series and shunt resistances describe the behavior of the PV module at the open-circuit conditions and at the short-circuit conditions, respectively. The solar irradiation current I_{ph} is represented by the current source and is defined as follows (Babu and Gurjar, 2014):

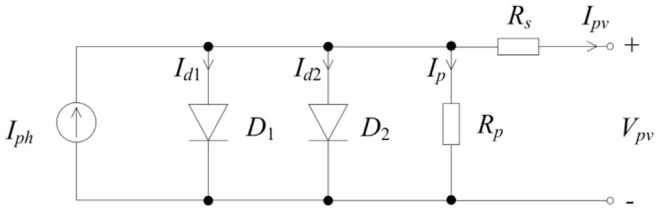

Fig. 1. Equivalent circuit of the standard two-diode model of the PV module.

$$I_{ph} = (I_{sc} + K_i \Delta T)\frac{G}{G_n} \tag{1}$$

where I_{sc} is the short-circuit current, K_i is the current temperature coefficient, G is the solar irradiation level in W/m^2, G_n is the nominal solar irradiation level (usually 1000 W/m^2), and ΔT is the difference between the module temperature and the nominal module temperature (usually 25 °C).

The PV module current in Fig. 1 is (Gupta et al., 2012)

$$\begin{aligned} I_{pv} &= I_{ph} - I_{01}\left(e^{\frac{V_d}{a_1 V_t}} - 1\right) - I_{02}\left(e^{\frac{V_d}{a_2 V_t}} - 1\right) - \frac{V_d}{R_p} \\ V_d &= V_{pv} + I_{pv} R_s \end{aligned} \tag{2}$$

where a_1 and a_2 are the diodes' ideality constants, and R_s and R_p are the PV module series and shunt resistances. These parameters were determined as in (Grgić et al., 2018).

The diodes' saturation currents are defined as follows (Gupta et al., 2012):

$$I_{01} = \frac{I_{sc} + K_i \Delta T}{e^{\frac{V_{ocn} + K_v \Delta T}{a_1 V_t}} - 1} \tag{3}$$

$$I_{02} = \frac{(T)^{\frac{2}{5}}}{3.77} I_{01} \tag{4}$$

Fig. 2 shows the equivalent circuit of the model proposed in (Grgić et al., 2018) in which the dynamic behavior of the PV module is modeled. The considered model is in fact the two-diode model expanded with the diodes' capacitances, which enable modeling of the dynamic behavior of the PV module. The capacitances in proposed model of the PV module are variable, so this model is called the variable-capacitance model.

The capacitances C_{j1} and C_{j2} represent the junction capacitance of the diodes D_1 and D_2, respectively. The junction capacitance comes from the charge stored in the depletion region at the semiconductor PN junction. It is dominant in the range of small negative and positive PV module voltages. The junction capacitance can be evaluated as (J. Millman and Halkais, 1972)

$$C_j(V_d) = \frac{C_{j0}}{N_s \sqrt{1 - \frac{V_d}{N_s \varphi_0}}} \tag{5}$$

where C_{j0} is the zero-voltage capacitance of the PV cell PN junction, φ_0 is the zero-voltage junction potential of the PV cell, and V_d is the voltage across diodes (φ_0 is the upper voltage bound for the model, so it should hold $\varphi_0 > V_{oc}$).

The magnitude of the junction capacitance depends on V_d value. The values of C_{j0} and φ_0 depend on the PV module construction material.

The capacitances C_{d1} and C_{d2} represent the diffusion capacitance of the diodes D_1 and D_2, respectively. The diffusion capacitance comes from the charge stored in the neutral region of the semiconductor, outside the depletion region. It is dominant in the range of high positive voltages, above the maximum power point voltage, where the junction carries significant current. The diffusion capacitance, which is dependent on the PV module temperature (T) and voltage (V_t) is given as (Kim et al., 2013)

$$C_d(T, V_d) = \frac{\tau I_d(T, V_d)}{a V_t(T)} \tag{6}$$

where τ is the mean carrier lifetime, I_d is the diode current.

The PV module current of the variable-capacitance model can be defined as (Grgić et al., 2018)

$$\begin{aligned} I_{pv} = I_{ph} &- I_{01}\left(e^{\frac{V_d}{a_1 V_t}} - 1\right) - I_{02}\left(e^{\frac{V_d}{a_2 V_t}} - 1\right) - \frac{V_d}{R_p} - \frac{d}{dt}\left(q_{j1} + q_{j2}\right. \\ &\left. + q_{d1} + q_{d2}\right) \end{aligned} \tag{7}$$

The PV module current I_{pv} in Eq. (7) consists of the static and dynamic parts. The first four terms on the right side of Eq. (7), i.e., the current source current, the diodes' currents, and the shunt resistance current, represent the static part of I_{pv}, whereas the last term on the right side of Eq. (7), i.e., the capacitors' currents, represent the dynamic part of the I_{pv}. In the variable-capacitance model, all four capacitances are variable. The junction and diffusion capacitor currents are, respectively (Grgić et al., 2018)

$$i_{cj} = \frac{dq_j}{dt} = \frac{dV_d C_j}{dt} = \left(C_j + V_d \frac{dC_j}{dV_d}\right)\frac{dV_d}{dt} = C_{jeff}\frac{dV_d}{dt} \tag{8}$$

$$i_{cd} = \frac{dq_d}{dt} = \frac{dV_d C_d}{dt} = \left(C_d + V_d \frac{dC_d}{dV_d}\right)\frac{dV_d}{dt} = C_{deff}\frac{dV_d}{dt} \tag{9}$$

In Eq. (8), the effective junction capacitance C_{jeff} is the sum of the static junction capacitance defined in Eq. (5) and the dynamic junction capacitance (right term in the bracket). Similarly, the effective diffusion capacitance C_{deff} is defined in Eq. (9).

The third considered model of the PV module is the constant-capacitance model of the PV module. This model has the same equivalent circuit as the variable-capacitance model, except that

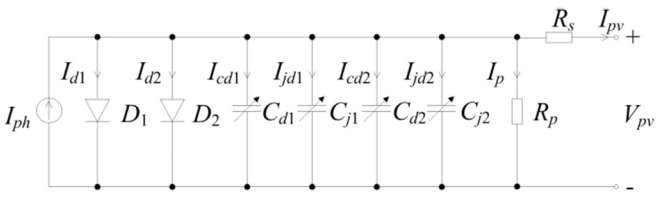

Fig. 2. Equivalent circuit of the variable-capacitance model of the PV module.

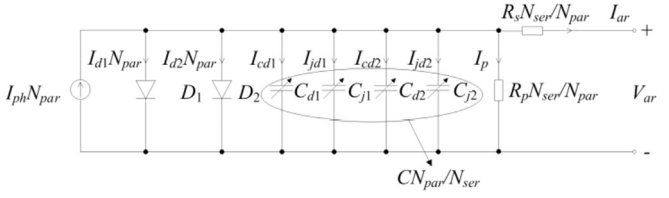

Fig. 3. Equivalent circuit of the variable-capacitance model of the PV array.

the variable capacitances are replaced by the constant capacitance. In this paper the constant capacitance value is $C_{con} = 5\ \mu F$, as in (Grgić et al., 2018).

2.2. Connecting of multiple PV modules

The values of voltage and current of a single PV module are generally too low for implementation with grid-tied inverters, so connecting of multiple PV modules is required. The series connection of the PV modules with the same characteristics increases the voltage and power, whereas the current stays the same. The parallel connection of the PV modules with the same characteristics increases the current and power, whereas the voltage stays the same. The serial connection of multiple PV modules is called the PV string, whereas the parallel connection of two or more strings is called the PV array. In Fig. 3 the equivalent circuit of the variable-capacitance model of the PV array is shown. V_{ar} represents the PV array voltage, I_{ar} represents the PV array current, N_{ser} represents the number of PV modules connected in series, and N_{par} represents the number of strings connected in parallel. The PV array considered in this paper consists of 2 strings, whereas each string consists of 16 PV modules.

The equivalent circuit of the standard two-diode model of the PV array is similar to the circuit shown in Fig. 3, except that it does not include the capacitances, whereas the equivalent circuit of the constant-capacitance model of the PV array contains a single constant capacitance instead of the variable capacitances.

3. The proposed system configuration

3.1. Quasi-Z-source inverter

The considered qZSI configuration shown in Fig. 4a consists of the impedance network and the three-phase inverter bridge with insulated-gate transistors and flywheel diodes. The impedance network consists of two inductors L_1, L_2, two capacitors C_1, C_2, and the diode D. At the impedance network input the PV array is connected with the additional input diode D_{in}, which inhibits negative PV array current, and additional input capacitor C_{in}, which inhibits rapid variations of the PV array voltage. The parasitic resistances of the qZSI inductors and capacitors (R_L and R_C, respectively) are included. For convenience, it is assumed $L_1 = L_2 = L$, $C_1 = C_2 = C$, $R_{L1} = R_{L2} = R_L$, $R_{C1} = R_{C2} = R_C$. The inductors L_f are inserted between the qZSI and the grid to filter the phase currents. The qZSI operates with the lower input dc voltage than the standard PWM inverter. This is made possible by introducing the additional switching state called the shoot-through (ST) state. During this state one or more inverter legs are short circuited and the voltage in the impedance network is boosted up. The considered qZSI utilizes the sine PWM with injected third harmonic voltage (Shen et al., 2006) and with the ST states embedded within the zero-state period. The boost factor B, the ST state period T_0, and the voltage gain G are given as

$$B = \frac{1}{1 - 2\frac{T_0}{T_{sw}}} = \frac{1}{1 - 2D_0} \tag{10}$$

$$T_0 = 2 \cdot N_0 \cdot T_s \tag{11}$$

$$G = \frac{\widehat{E}_{ac}}{V_{in}/2} = M \cdot B \tag{12}$$

where T_{sw} is the switching period of the inverter, T_s is the sampling period, M is the modulation index, N_0 is the ST duration factor, $\widehat{E}_{ac}$ is the magnitude of the fundamental harmonic of the grid phase voltage, V_{in} is the qZSI's input dc voltage, and D_0 is the ST duty ratio.

The ST duration factor (N_0) is a positive integer which defines the duration of the ST state depending on the sampling period (T_s). Consequently, the control of the duty ratio (D_0) depends on N_0, T_s, and switching period (T_{sw}). For the sampling periods $T_s > 10\ \mu s$ the changes of N_0 cause big step changes of D_0 so precise control of D_0 is not viable. Therefore, achieving precise control of D_0 implies either a powerful microprocessor and expensive hardware setup or switching frequencies of the order of a few kHz.

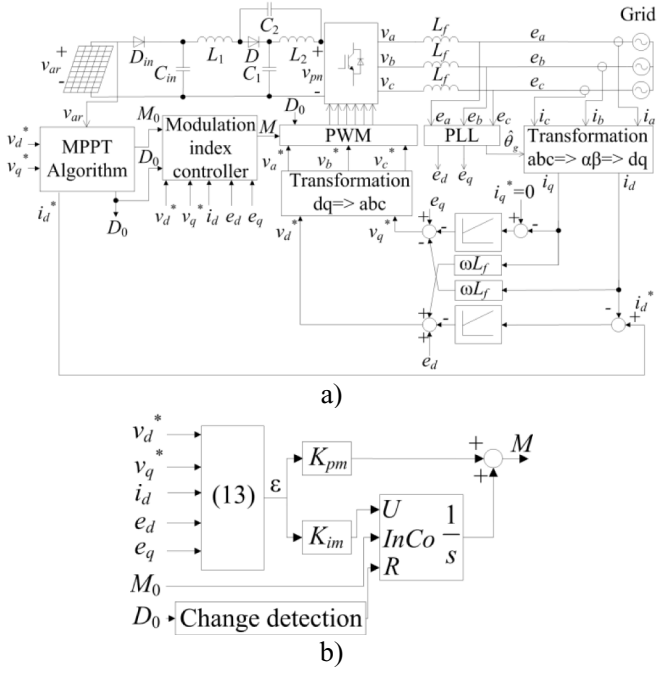

Fig. 4. (a) Structure of the proposed PV-qZSI control system, (b) modulation index PI controller.

3.2. Inverter-grid synchronization

The main tasks of the qZSI control system in Fig. 4a are to synchronize the qZSI with the grid and to ensure the PV array operates in MPP. The phase locked loop (PLL) synchronizes the qZSI with the grid by tracking the magnitude and the phase of the grid voltage vector, whereas the MPPT algorithm tracks the PV array MPP. The considered qZSI control system is implemented in the direct-quadrature (dq) coordinate system, which enables control of the power factor through control of the reference axis currents (i_d^*, i_q^*). The reference d-axis current (i_d^*) determines the active power injected to the grid, whereas the reference q-axis current (i_q^*) determines the reactive power injected to the grid. In this paper, the desired power factor is 1 ($i_q^* = 0$), whereas i_d^* is calculated by the MPPT algorithm.

The modulation index PI controller is shown in Fig. 4b. The error signal (ε) of the PI controller in Eq. (13) is obtained based on the vector diagram of the ac-side voltages and currents. The integrator of the modulation index PI controller has the reset signal (R) and the initial condition signal ($InCo$).

$$\varepsilon = \sqrt{\left(v_d^*\right)^2 + \left(v_q^*\right)^2} - \sqrt{e_d^2 + e_q^2 + \left(i_d \cdot \omega \cdot L_f\right)^2} \tag{13}$$

The change of the ST duty ratio D_0 resets the integrator to the initial modulation index (M_0). The calculation of D_0 and M_0 is

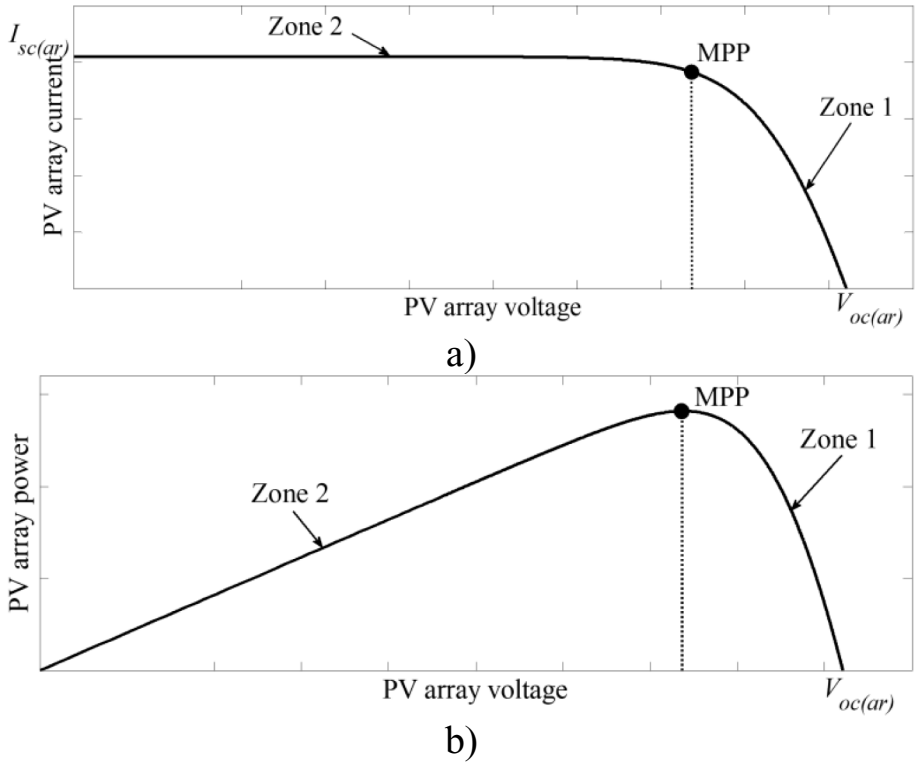

Fig. 5. (a) PV array static I-V characteristic, (b) PV array static P-V characteristic.

explained in the next section.

4. Proposed maximum power point tracking algorithm

The proposed MPPT algorithm controls three qZSI variables: the reference d-axis current (i_d^*), the ST duty ratio (D_0), and the initial value of the modulation index (M_0). The characteristic in Fig. 5a shows that small change of the PV array current in Zone 1 causes small change of the PV array voltage, whereas in Zone 2 the opposite is true. Consequently, oscillations of the PV array current in Zone 2 cause significant variations in the PV array voltage and ultimately the PV array operating point may come near the short-circuit point, which would lead to lower than required qZSI input voltage. Considering these facts the operation of the PV array in Zone 2 is undesirable. The characteristic in Fig. 5b shows that the PV array voltage reduction in Zone 1 causes the increase of the PV array power, whereas in Zone 2 the opposite holds.

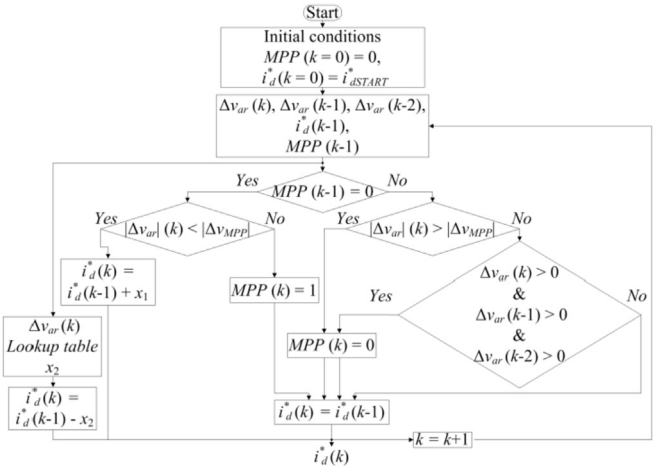

Fig. 6. Flow chart of the control of the reference d-axis current in the proposed MPPT algorithm.

In the proposed system the d-axis current (i_d) follows the reference d-axis current (i_d^*) and determines the PV array current in Zone 1, since the PV array voltage change in that zone is small. As the operating point approaches Zone 2, the PV array voltage changes become larger. Hence, the proposed MPPT algorithm increases i_d^* while the operation point is in Zone 1 and based on the PV array voltage changes detects the MPP, as explained below.

Fig. 6 shows the flow chart of the i_d^* control in the proposed MPPT algorithm, whose main tasks are to reach the MPP of the PV array and to ensure stable system operation. The input variables of the flow chart are the values of the PV array voltage change (Δv_{ar}) at instants k, k-1, k-2, the value of i_d^* from the previous step, and the value of the MPP detection signal from the previous step (if MPP (k-1) = 1, MPP is achieved; if MPP (k-1) = 0, MPP is not achieved). The MPPT algorithm is activated after the PV array is connected to the grid through the qZSI and the steady-state is achieved. At the start of the MPPT algorithm, the MPP detection signal is zero ($MPP = 0$) and the search for the optimal i_d^* value is initiated from the current i_d^* value (i_{dSTART}^*). The MPPT algorithm increases i_d^* in equal increments (x_1) until the MPPT algorithm detects $|\Delta v_{ar}(k)| > |\Delta v_{MPP}|$, ($\Delta v_{MPP}$ is the zone crossing threshold, i.e., the PV array voltage change for which the crossing from Zone 1 to Zone 2 is detected). This means that the MPP is reached ($MPP = 1$) and i_d^* is decreased for the value x_2 which is determined by the lookup table (given in Appendix), to ensure operation in Zone 1 (Fig. 5). After the MPP is reached, i_d^* does not change until the change of the solar irradiation or the PV array temperature is detected. For constant i_d^*, the solar irradiation level change or the PV array temperature change affect the PV array voltage. The PV array temperature changes much slower than the solar irradiation level. Supposing

Table 1
ST duty ratio settings.

Condition	ST duty ratio
$v_{ar}(k\text{-}1) < 515\,V$ & $v_{ar}(k) \geq 515\,V$	$D_0 = 0.25$
$v_{ar}(k\text{-}1) > 470\,V$ & $v_{ar}(k) \leq 470\,V$	$D_0 = 0.3$
$v_{ar}(k\text{-}1) < 410\,V$ & $v_{ar}(k) \geq 410\,V$	$D_0 = 0.3$
$v_{ar}(k\text{-}1) > 360\,V$ & $v_{ar}(k) \leq 360\,V$	$D_0 = 0.35$
$v_{ar}(k\text{-}1) < 320\,V$ & $v_{ar}(k) \geq 320\,V$	$D_0 = 0.35$
$v_{ar}(k\text{-}1) > 290\,V$ & $v_{ar}(k) \leq 290\,V$	$D_0 = 0.4$

the PV temperature is constant, if $MPP\ (k\text{-}1) = 1$ and ($|\Delta v_{ar}\ (k)| > |\Delta v_{MPP}|$), the solar irradiation level decrease is detected. Consequently, i_d^* is decreased for the value which is determined by the lookup table and the MPPT algorithm tracks the new MPP ($MPP\ (k) = 0$). Otherwise, if $MPP\ (k\text{-}1) = 1$ and the values of Δv_{ar} at instants k, k-1, and k-2 are all greater than 0 V, the solar irradiation level increase is detected and the MPPT algorithm tracks the new MPP ($MPP\ (k) = 0$).

If the solar irradiation is assumed constant, if $MPP\ (k\text{-}1) = 1$ and ($|\Delta v_{ar}\ (k)| > |\Delta v_{MPP}|$), the PV array temperature is increased. Consequently, i_d^* is decreased for the value which is determined by the lookup table and the MPPT algorithm tracks the new MPP ($MPP\ (k) = 0$). Otherwise, if $MPP\ (k\text{-}1) = 1$ and the values of Δv_{ar} at instants k, k-1, and k-2 are all greater than 0 V, the PV array temperature decrease is detected and the MPPT algorithm tracks the new MPP ($MPP\ (k) = 0$).

In the considered qZSI configuration, according to Eqs. (10)–(12), the desired voltage gain can be achieved by variation of the modulation index (M) or the ST duty ratio (D_0). The modulation index (M) is limited with respect to D_0 according to the maximum constant boost strategy (MCBS) in (Shen et al., 2006). Table 1 shows the ST duty ratio settings with respect to the PV array voltage value (v_{ar}). The values used in Table 1 were determined based on the sampling frequency and the switching frequency given in Section 5.

Each step change of D_0 causes transients in M. To alleviate this, the integrator of the modulation index PI controller is set to the initial value defined in Eq. (14) when a change in D_0 occurs. In Eq. (14) following from Eq. (12), the initial modulation index value (M_0) is calculated in dependence of the reference voltages of the qZSI (v_d^*, v_q^*), the boost factor (B), and the PV array voltage (v_{ar}).

$$M_0 = \frac{2 \cdot \sqrt{\left(v_d^*\right)^2 + \left(v_q^*\right)^2}}{B \cdot v_{ar}} \tag{14}$$

Table 2
PV module parameters.

Parameters	Values
Open-circuit voltage, V_{oc}	34.78 V
Short-circuit current, I_{sc}	7.77 A
D_1 ideality constant, a_1	1.4
D_2 ideality constant, a_2	2
Series resistance, R_s	0.35 Ω
Shunt resistance, R_p	250.15 Ω
Number of series connected cells, N_s	60
Voltage temperature coefficient, K_v	−128.7 mV/°C
Current temperature coefficient, K_i	4.355 mA/°C
Zero-voltage capacitance, C_{j0}	11.7 μF
Zero-voltage junction potential, φ_0	0.82 V
Mean carrier lifetime, τ	5.76 μs
Constant capacitance, C_{con}	5 μF
Input capacitance, C_{in}	470 μF
Number of series connected PV modules in a string, N_{ser}	16
Number of parallel connected strings, N_{par}	2
MPPT algorithm sampling frequency, f_{MPP}	10 Hz
i_d^* increment, x_1	0.1 A
Zone crossing threshold, Δv_{MPP}	−5 V

Table 3
qZSI parameters.

Parameters	Values
qZSI inductance, L	From Eq. (15)
qZSI capacitance, C	20 μF
qZSI inductors parasitic resistance, R_L	500 mΩ
qZSI capacitors parasitic resistance, R_C	125 mΩ
PWM switching frequency, f_{sw}	2 kHz

Table 4
Minimum and maximum absolute deviation from MPP.

Temperature	Novel MPPT algorithm		CV MPPT algorithm	
	Min	Max	Min	Max
25 °C	178 W	222 W	242 W	342 W
50 °C	127 W	205 W	0 W	197 W
75 °C	83 W	220 W	618 W	673 W

5. Results and discussion

Simulation model of the system under consideration was built in MATLAB Simulink. For this purpose, the simulation model of the qZSI from (Bašić et al., 2017) and the simulation model of the PV module from (Grgić et al., 2018) were unified and the proposed MPPT algorithm was implemented. The saturation of the inductors in the impedance network of the qZSI was taken into account as in (Bašić et al., 2017)

$$L_{eff} = \frac{1.64}{81.01 + I_L^2} \tag{15}$$

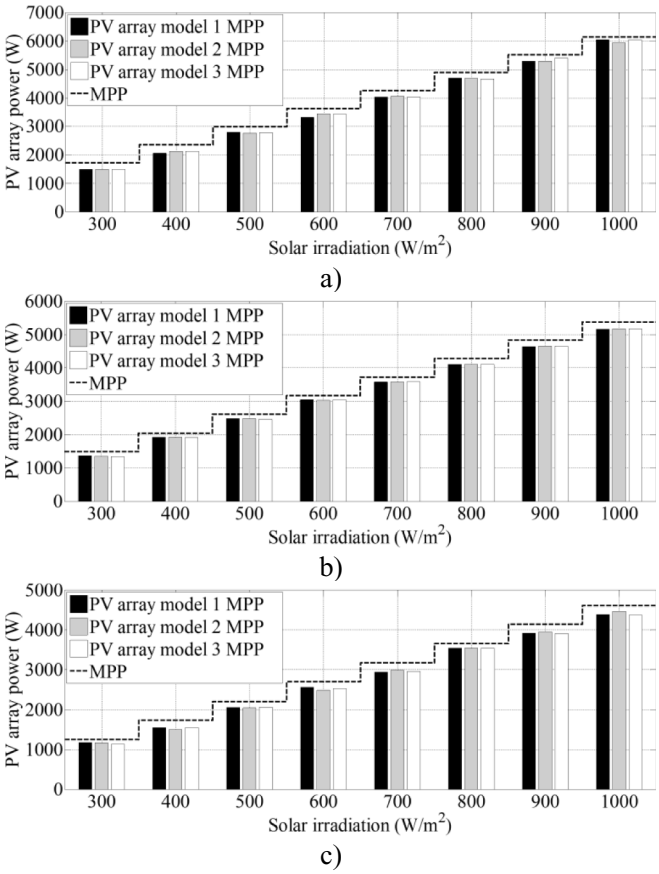

Fig. 7. PV array power vs. solar irradiation, for the different models of the PV array, and the PV array temperatures: (a) $T = 25$ °C, (b) $T = 50$ °C, (c) $T = 75$ °C.

The simulation input parameters for the monocrystalline PV module SV60-235E produced by Solvis are summarized in Table 2. The PV module parameters were determined from the experimentally obtained I-V characteristics. The measurements were carried on the actual PV module SV60-235E installed on the roof of the building, as reported in (Grgić et al., 2018). The input parameters of the qZSI are summarized in Table 3. The root mean square value of the grid voltage is $E_{ac} = 230$ V. In the simulation model the sampling frequency of 10 kHz was used for all the segments apart from the MPPT (10 Hz) and the SPWM signal generation (80 kHz) (See. Table 4).

Figs. 7–10 show the obtained simulation results. In these figures, PV array model 1 denotes the standard two-diode model of the PV array, PV array model 2 denotes the variable-capacitance model of the PV array, whereas PV array model 3 denotes the constant-capacitance model of the PV array.

5.1. Steady-state analysis

Fig. 7 shows the PV array MPPs at different solar irradiation levels and PV array temperatures. Dashed line represents the theoretical MPPs, obtained from the PV array static P-V characteristics, whereas the bars represent the MPPs achieved in the simulations. The MPPs achieved with all the considered models of the PV array have good fitting with the dashed line MPPs, although there are minor discrepancies caused by the differences in the PV array models.

Fig. 8 shows the percentage deviations from the theoretical MPP for each considered model of the PV array, for different solar irradiation levels and PV array temperatures. The deviations depend on the utilized model of the PV array and vary with both the solar irradiation level and the PV array temperature. For the PV array temperature $T = 25$ °C (Fig. 8a), the deviations from the theoretical MPP increase with the reduction of the irradiation. The same trend

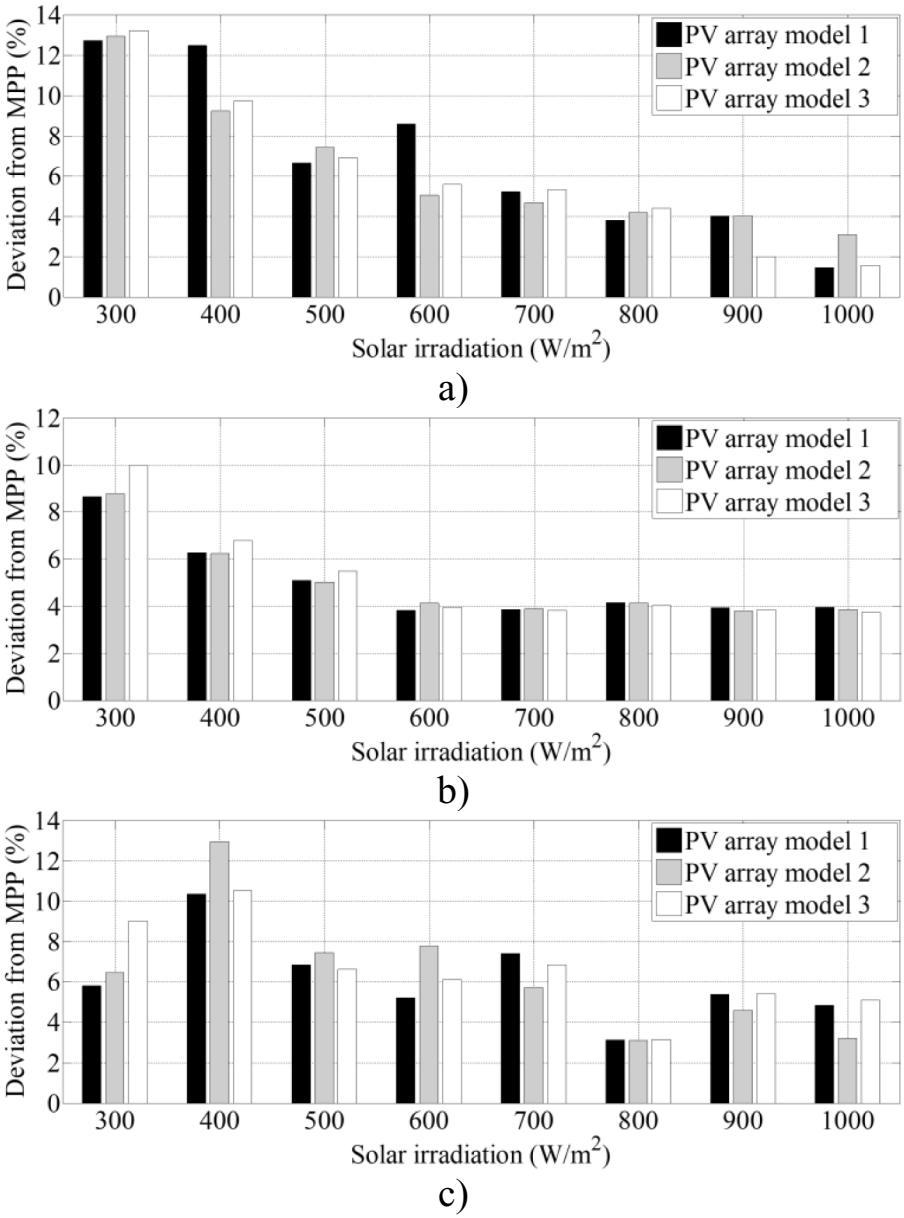

Fig. 8. Deviation from MPP vs. solar irradiation for the different models of the PV array, and the PV array temperatures: a) $T = 25$ °C, b) $T = 50$ °C, c) $T = 75$ °C.

is present for the PV array temperature $T = 50\,°C$ (Fig. 8b), whereas for the PV array temperature $T = 75\,°C$ (Fig. 8c) the deviations do not have a pronounced trend.

With the assumption that the variable-capacitance model of the PV array best describes the behavior of the actual PV array (Kim et al., 2013) it is here used as the reference model for comparison. The greatest deviation in the MPP between the standard two-diode model and the variable-capacitance model occurs at the solar irradiation level 600 W/m^2 and the PV array temperature $T = 25\,°C$. In that point the power production in the standard two-diode model is 128 W lower compared to the variable-capacitance model. On the other hand, the greatest deviation in the MPP between the constant-capacitance model and the variable-capacitance model occurs at the solar irradiation level 1000 W/m^2 and the PV array temperature $T = 75\,°C$. In that point the power production in the constant-capacitance model is 87 W lower compared to the variable-capacitance model.

5.2. Dynamic analysis

Fig. 9 shows the time responses of the PV array variables for different solar irradiation levels and constant PV array temperature of 75 °C. The PV array power is shown in Fig. 9a. The indicated solar irradiation step changes in Fig. 9a apply for Figs. 9 and 10 as well. At $t = 0$ s the qZSI is connected to the grid, whereas at $t = 1$ s the MPPT algorithm is activated. At $t = 2.15$ s the MPP for the solar irradiation level 1000 W/m^2 is reached. The solar irradiation step change from 1000 W/m^2 to 500 W/m^2 occurs at $t = 5$ s. Consequently, the PV array power drops and at $t = 7.3$ s the MPP for the solar irradiation 500 W/m^2 is reached. At $t = 10$ s, the solar irradiation step change from 500 W/m^2 to 800 W/m^2 occurs and at $t = 13.5$ s the MPP for the solar irradiation 800 W/m^2 is reached. Fig. 9b shows the PV array current with the indicated transients, whereas Fig. 9c shows the PV array voltage. The changes of the PV array current and the PV array voltage have the opposite trend because the PV array operating points are in Zone 1 (Fig. 5a). The PV array voltage changes during transients may reach 170 V. However, the respective steady-state values differ for only about 5 V. Greater changes of the steady-state values are expected for the PV array temperature changes, but these are much slower compared to the solar irradiation changes, so they are not considered in the dynamic analysis.

In Fig. 9b the transients of the PV array current are indicated for the moments when the PV array reaches the MPP for different solar irradiation levels. For the variable-capacitance model of the PV array, the PV array current exhibits overshoot for all three indicated transients, whereas for the other two considered models, the PV current exhibits overshoots for two out of three transients. The differences between the responses obtained for different models of the PV array are due to the different dynamic behavior of each model. Fig. 9d shows the change of the PV array capacitances for the variable-capacitance model. The equivalent junction capacitance (sum of D_1 and D_2 junction capacitances in Fig. 3) is about fifteen times lower than equivalent diffusion capacitance (sum of D_1 and D_2 diffusion capacitances in Fig. 3), so the influence of the equivalent junction capacitance is practically negligible in this study. The capacitances vary similar to the PV array voltage (Fig. 9c), because the capacitances are defined as function of the PV array voltage.

Fig. 9e shows the reference d-axis current (i_d^*), which is obtained at the output of the MPPT algorithm. During the system startup, the reference d-axis current is set to a constant initial value ($i_{dSTART}^* = 7.8$ A), which was selected in order to shorten the initial MPP search. At $t = 1$ s the MPPT algorithm starts to increase i_d^*, whereas at $t = 2.15$ s the MPPT algorithm detects the MPP and keeps i_d^* at a constant value which is maintained until the solar irradiation level changes. At $t = 5$ s, the MPPT algorithm detects $|\Delta v_{ar}(k)| > |$

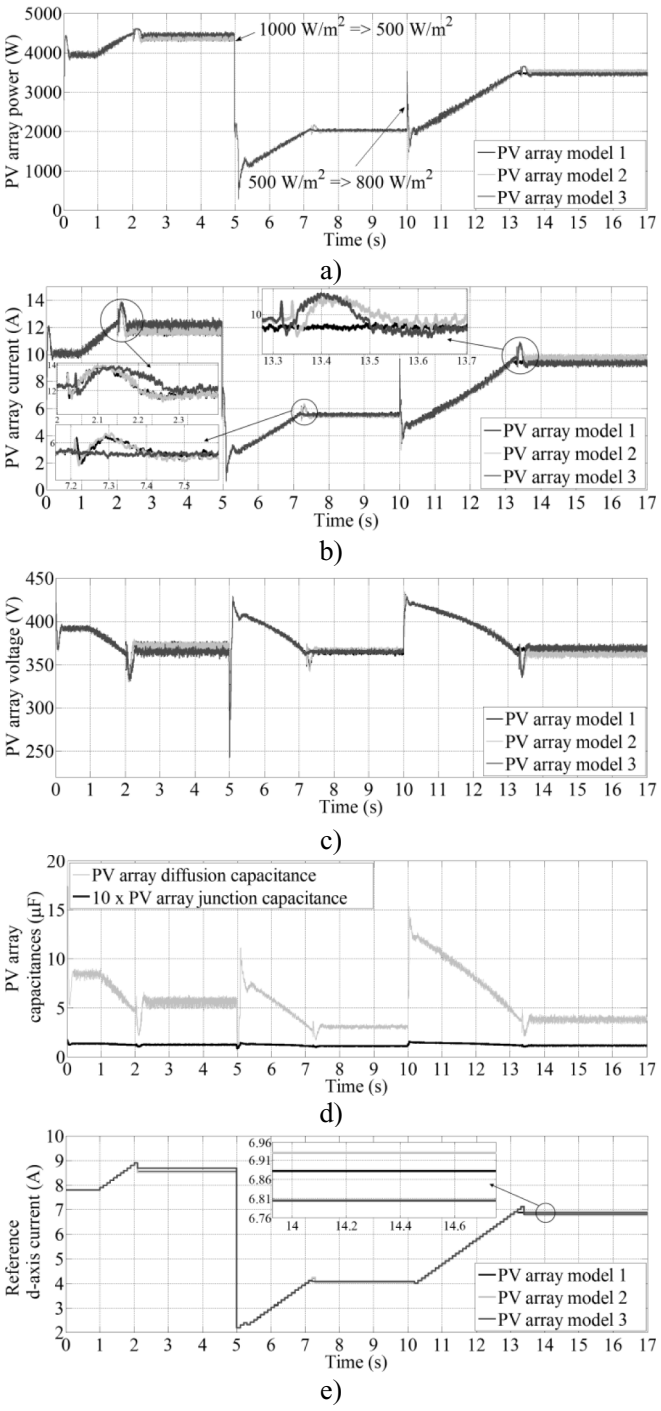

Fig. 9. Variables of the PV array for different solar irradiation levels and the constant PV array temperature (75 °C): (a) power, (b) current, (c) voltage, (d) capacitances, (e) reference d-axis current.

$\Delta v_{MPP}|$ and decreases i_d^* according to the lookup table (Appendix). In the next step the MPPT algorithm starts to increase i_d^* to reach the MPP for the present solar irradiation level, which is accomplished at $t = 7.3$ s. Further, at $t = 10$ s, MPPT algorithm detects positive Δv_{ar} for three consecutive instants and starts to increase i_d^* to reach the new MPP, which is achieved at $t = 13.4$ s. The reference current i_d^* steady-state value depends on the model of the PV array. The zoomed area in Fig. 9e shows the steady-state values of i_d^* obtained for the solar irradiation level 800 W/m^2. At this particular point the maximum difference in i_d^* is between the variable-capacitance

model and the constant-capacitance model of the PV array and amounts to 0.15 A, which implies the difference in the PV array power production of about 70 W in favor of the variable-capacitance model (Fig. 9a).

Fig. 10 shows the characteristic variables of the qZSI for different solar irradiation levels and constant PV array temperature. The time responses in Fig. 10 are shown only for the variable-capacitance model, whereas similar responses were obtained for the other two models. Fig. 10a shows the modulation index (M) and the ST duty ratio (D_0). The modulation index varies from 0.55 to 0.8, and has the opposite trend than the PV array voltage (Fig. 9c). D_0 changes to maintain M in the limits defined by the MCBS, so when the PV array voltage drops below the allowed lower limit, D_0 is increased according to Table 1. Conversely, when the PV array voltage rises above the allowed upper limit, D_0 is decreased. Fig. 9b shows that the actual d-axis current (i_d) closely tracks the reference d-axis current (i_d^*) but this comes at the cost of a relatively large ripple of i_d. At $t = 5$ s due to the solar irradiation step change the reference d-axis current was decreased to $i_d^* = 2.2$ A. This is the lowest allowed value of i_d^* because below this value the currents of the inductors in the impedance network of qZSI rise during non-ST states as well. Consequently, the voltages across the impedance network capacitors increases (Shen and Peng, 2008). Given the fact that the power obtainable from the considered PV array under this circumstances is only about 1 kW (the power injected to the grid is further reduced by qZSI losses), this minimum current does not represent a significant limitation in the operation of the system. Finally, Fig. 10c shows the phase current and voltage. The phase shift between the phase current and voltage is zero, which means that the qZSI injects only the active power to the grid. Total harmonic distortion (THD) of the current shown in Fig. 10c was determined to be 25.3%. The THD could be improved by increasing the switching frequency but, at the same time, the precision of D_0 adjustment would be reduced, thus inducing oscillations in the PV array voltage and deteriorating the performance of the MPPT algorithm. Alternatively, the THD value could be reduced by increasing the inductance of the qZSI inductors, but at the expense of increasing the size and cost of the qZSI.

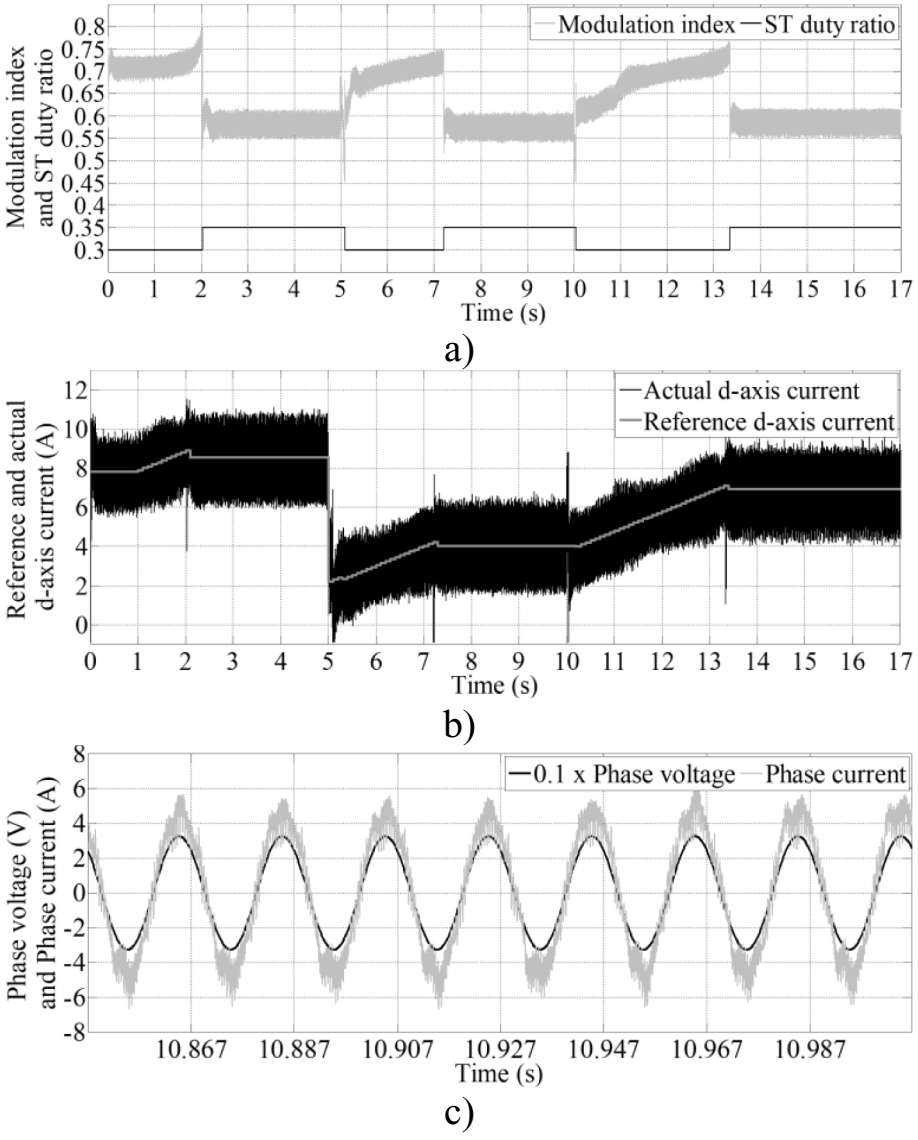

Fig. 10. Characteristic variables of the qZSI for different solar irradiation levels and the constant PV array temperature: (a) Modulation index, ST duty ratio, (b) Reference and actual d-axis current, (c) Phase current and voltage.

5.3. Performance comparison of the proposed MPPT algorithm and conventional CV algorithm

The performance of the proposed MPPT algorithm is in this section compared with that of the conventional CV algorithm. The CV algorithm was chosen for comparison due to the fact that it also requires only measurement of the PV array output voltage, as opposed to other competing algorithms which require additional measurements. Fig. 11 shows the results obtained for the two considered algorithm in terms of deviation of the obtained PV array power from the actual MPP. The results encompass solar irradiances in the range 300 W/m^2 – 1000 W/m^2 and PV array temperatures in the range 25 °C – 70 °C. The CV algorithm is designed to ensure maximum PV array power at 1000 W/m^2 (maximum irradiance level) and 50 °C (average PV array operating temperature). Consequently, the deviation from the actual MPP is zero for these conditions in Fig. 11. . The deviation of the CV algorithm, however, steadily increases by reducing the solar irradiation level so, even at this temperature; it exceeds the deviation of the proposed algorithm for irradiations lower than 600 W/m^2. At other considered temperatures, the proposed MPPT algorithm results in smaller deviations compared to the CV algorithm over the whole irradiance range. These differences are particularly pronounced at $T = 75$ °C.

The minimum and maximum absolute deviations obtained for the considered algorithms are provided in Table 3. For the proposed algorithm, the maximum deviation noted amounted to 222 W, whereas for the CV algorithm, it reached 673 W. The CV algorithm offered better performance only at $T = 50$ °C – i.e., the operating temperature for which it was originally designed.

6. Conclusion

In this paper the control system of the grid-tied qZSI in the PV application is proposed. The proposed MPPT algorithm does not require the measurement of the PV array current and there are no oscillations around the MPP. The MPP is successfully tracked by

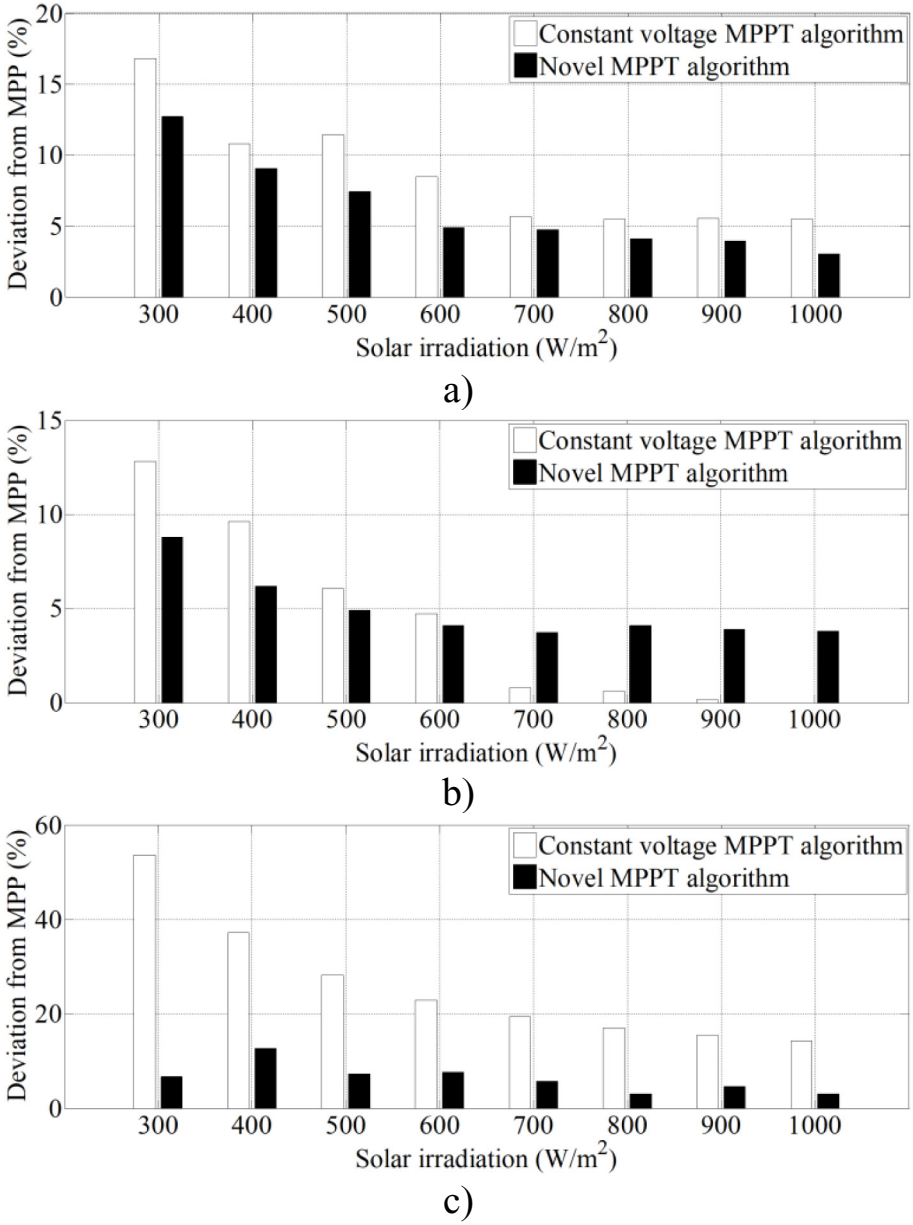

Fig. 11. Deviation from the MPP vs. solar irradiation level for the proposed MPPT algorithm and constant-voltage algorithm: a) $T = 25$ °C, b) $T = 50$ °C, c) $T = 75$ °C.

changing the reference d-axis current on the grid side, whereas the stable operation of the considered system is ensured by changing the ST duty ratio in discrete steps. The operation of the proposed MPPT algorithm is tested for the solar irradiation level range from 300 W/m^2 to 1000 W/m^2 and the PV array temperature range from 25 °C to 75 °C. The available PV array power below the minimum considered irradiation level becomes rather small, i.e., less than 1 kW according to Fig. 7. By considering the losses of the qZSI inverter, there would be very little power left for the grid. The actual system should probably be disconnected from the grid under this scenario due to low efficiency.

The simulation results show that the proposed MPPT algorithm has efficiency which is comparable to that reported in literature. For example, for the solar irradiation level 300 W/m^2 the efficiency is 90%, whereas for the solar irradiation level 1000 W/m^2 the efficiency is 97%. The performance of the proposed MPPT algorithm has been compared to that of the conventional CV algorithm. It was observed that the proposed algorithm provides up to 453 W more power from the PV array (i.e., about 7% of the respective nominal power) within the considered operating range. Any improvement in this respect increases the cost-effectiveness of the system, especially in the long run, and also contributes to overall increase in the electrical energy obtained from clean energy sources, thus reducing the use of fossil fuels and CO2 emissions.

During the testing of the MPPT algorithm, three different models of the PV array were used. One of them does not describe the dynamic behavior of the PV array, whereas the other two models describe the dynamic behavior by introducing the constant or variable capacitances. The influence of the capacitances on the efficiency of the proposed MPPT algorithm is significant. The greatest observed deviation in the achieved MPPs between the considered models of the PV array was shown to exceed 100 W. There are also differences in the PV array transient responses between the considered models. Namely, the PV array variables of the variable-capacitance model, unlike the other two models, exhibit overshoot for all the considered transients. Considering these facts, it is important to include the dynamic behavior into the model of the PV array, because it has influence on the MPPT algorithm performance. In the future, it is planned to experimentally test the proposed configuration and to introduce the batteries into the proposed system configuration.

Acknowledgment

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Appendix

Table A.1
Values of i_d^* decrements x_2

Δv_{ar} (V)	x_2 (A)
- 5	0.025
- 6	0.05
- 8	0.075
- 10	0.1
- 12	0.125
- 14	0.15
- 16	0.2
- 18	0.25
- 20	0.3
- 25	0.35
- 30	0.4
- 40	2

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Znanstveni rad III

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Calculation of Semiconductor Power Losses of a Three-Phase Quasi-Z-Source Inverter

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Abstract: This paper presents two novel algorithms for the calculation of semiconductor losses of a three-phase quasi-Z-source inverter (qZSI). The conduction and switching losses are calculated based on the output current-voltage characteristics and switching characteristics, respectively, which are provided by the semiconductor device manufacturer. The considered inverter has been operated in a stand-alone operation mode, whereby the sinusoidal pulse width modulation (SPWM) with injected 3rd harmonic has been implemented. The proposed algorithms calculate the losses of the insulated gate bipolar transistors (IGBTs) and the free-wheeling diodes in the inverter bridge, as well as the losses of the impedance network diode. The first considered algorithm requires the mean value of the inverter input voltage, the mean value of the impedance network inductor current, the peak value of the phase current, the modulation index, the duty cycle, and the phase angle between the fundamental output phase current and voltage. Its implementation is feasible only for the Z-source-related topologies with the SPWM. The second considered algorithm requires the instantaneous values of the inverter input voltage, the impedance network diode current, the impedance network inductor current, the phase current, and the duty cycle. However, it does not impose any limitations regarding the inverter topology or switching modulation strategy. The semiconductor losses calculated by the proposed algorithms were compared with the experimentally determined losses. Based on the comparison, the correction factor for the IGBT switching energies was determined so the errors of both the algorithms were reduced to less than 12%.

Keywords: loss-calculation algorithm; power inverter losses; quasi-Z-source inverter; semiconductor losses

1. Introduction

The growing production of the electrical energy from renewable sources requires new solutions in the field of power inverters. Conventional voltage-source inverters (VSIs) in applications with photovoltaic modules or fuel cells usually require an additional dc-dc boost converter. The main task of this converter is to boost and control the input voltage. One of the possible alternatives is to use single stage buck-boost inverters, such as the Z-source inverter (ZSI) [1,2]. This inverter boosts the input voltage by short circuiting one or more inverter phase legs, thus achieving the so-called shoot-through (ST) state. Many modifications and improvements have been proposed for the ZSI topology [2,3], as well as for the respective switching modulation strategies [4]. The quasi-ZSI (qZSI) topology [5] is probably the most widely used modification of the ZSI topology. The main advantages of the qZSI are continuous input current and reduced voltage rating of one of the capacitors in the impedance network. The main disadvantages of the Z-source-related topologies compared to the combination of the dc-dc boost converter and VSI are the lower efficiency [6] and the electromagnetic interference and safety problems due to the leakage current [7].

Inverter power losses are an important factor in inverter analysis. These losses consist of semiconductor and passive component losses. The calculation of the latter is rather simple, whereas the calculation of the semiconductor losses is much more complex, and many methods have been proposed to deal with it. Methods in [8–10] calculate the semiconductor losses based on the measured voltage and current of the respective semiconductor devices. These methods are prone to measurement errors. In addition, a current sensor should preferably be installed in each leg of an inverter because otherwise an asymmetry in the inverter legs' conductance could occur. On the other hand, methods in [6,11–22] are based on the output current-voltage (I–V) characteristics and switching characteristics provided by the semiconductor device manufacturer. The loss-calculation algorithms proposed in [6,11–19] require the mean and the root mean square (RMS) values of the currents and voltages of an inverter and are applicable only for one [11–13] or few similar topologies [6,14–16] and for a specific switching modulation strategy. The algorithms presented in [20,21] are based on instantaneous values of the currents and voltages of an inverter and are more generally applicable. The accuracy and the implementation of the mentioned algorithms highly depend on the amount of detail provided in the semiconductor device datasheet (i.e., the output I–V characteristics and switching characteristics vs. the junction temperature or the collector-emitter voltage).

The calculation of semiconductor losses of the previously mentioned ZSI and qZSI topologies represents a challenging task. The loss-calculation algorithms designed for the conventional VSI in [11–13] may not be used for the ZSI topologies since in the latter case there are additional losses produced by the ST states. Furthermore, losses of the diode in the ZSI impedance network also have to be accounted for. Algorithms in [6,14,15] calculate both the conduction and switching losses of the ZSI. However, the authors in [6] have considered the relationship between the semiconductor current and switching energies to be linear. More accurate approximation is ensured by utilizing the characteristics provided by the semiconductor device manufacturer [14,15]. As for the qZSI, the semiconductor losses in [10] were calculated according to the measured current and voltage of the respective semiconductor devices. However, these measurements have to be made very accurately, because even low measurement errors, due to the multiplication of the instantaneous voltage and current, could result with high loss calculation errors. The authors in [17] proposed the semiconductor loss-calculation algorithm (LCA) for the current-fed qZSI, whereas in [18,19] the same was done for the voltage-fed qZSI. However, in the three mentioned papers, the relationship between the semiconductor current and switching energies is considered to be linear. Finally, in [6,17–19] the switching losses were calculated without considering the impact of the phase angle between the fundamental output phase current and voltage. This impact was considered in [14,15], but only for the traditional PWM switching states and not for the ST states.

This paper considers the semiconductor power losses of the qZSI with implemented sinusoidal pulse width modulation (SPWM) with injected 3rd harmonic. Two proposed LCAs calculate the losses of the impedance network diode and the losses of the insulated-gate bipolar transistors (IGBTs) and free-wheeling diodes (FWDs) in the inverter bridge. In the case of the IGBTs, the conduction losses and the switching (turn-on and turn-off) losses were calculated, whereas in the case of the diodes, the conduction and reverse recovery losses were calculated. Both the proposed LCAs require the output I-V characteristics and the switching characteristics provided by the semiconductor device manufacturer. The first considered LCA (LCA1) is based on the algorithms presented in [11–13], which were there applied for the conventional VSI. However, unlike the conventional VSI, the qZSI utilizes the additional ST states, whose losses also need to be calculated. The input variables of the LCA1 are the mean value of the qZSI input voltage and current, the peak value of the output phase current, the duty cycle, the modulation index, and the phase angle between the fundamental output phase current and voltage. On the other hand, the second LCA (LCA2) is based on the algorithm presented in [20,21], but here it is adapted for the qZSI in order to account for the ST states. The input variables of the LCA2 are the instantaneous values of the following variables: the inverter input voltage and current, the impedance network diode current, the duty cycle, and the inverter output phase current.

The semiconductor losses calculated by the two proposed LCAs are compared with the experimentally determined losses, obtained for different values of the switching frequency, input voltage, ST duty cycle, and phase current. The semiconductor losses were experimentally determined by subtracting the measured qZSI output power and the calculated losses of the impedance network inductors from the measured qZSI input power, whereas the losses of the impedance network capacitors were neglected.

2. Quasi-Z-Source Inverter Power Losses

The considered stand-alone control system with the qZSI is shown in Figure 1. In this study, a symmetrical impedance network is considered, i.e., $L_1 = L_2 = L$, $C_1 = C_2 = C$, and $R_{L1} = R_{L2} = R_L$. The additional LCL filter, composed of the inductors (L_{f1}, L_{f2}), capacitors (C_f), and damping resistances (R_d), is connected at the inverter output. The considered qZSI supplies the three-phase resistive load (R_{ac}), whereby the control system maintains the required RMS value of the fundamental load phase voltage (V_{ac}) through adjustment of the modulation index (M). The SPWM with injected 3rd harmonic has been implemented. The qZSI utilizes the standard SPWM switching states (also known as the non-ST states) along with the ST states. The latter occur at the beginning of each zero-switching state of the SPWM, i.e., twice within each switching period (T_{sw}), in order to provide the required input voltage boost

$$B = \frac{1}{1-2D} = \frac{1}{1-2\frac{T_0}{T_{sw}}} \tag{1}$$

where D is the ST duty cycle and T_0 is the ST state period.

The peak value of the load phase voltage ($V_{ac,pk}$) and the peak value of the inverter bridge input voltage (V_{pn}) may be defined as follows:

$$\begin{aligned} V_{ac,pk} &= BM\frac{V_{in}}{2} \\ V_{pn} &= BV_{in} = \frac{V_{in}}{1-2D} \end{aligned} \tag{2}$$

where V_{in} represents the qZSI input voltage.

The power losses of the qZSI are defined as the difference between the inverter input and output power. These losses may be divided into the semiconductor losses, the core losses of the impedance network inductors, and the parasitic resistance losses. In this study, the latter losses include only the copper losses of the impedance network inductors, whereas the power losses of the impedance network capacitors are considered negligible due to the low equivalent series resistance (ESR) of the utilized polypropylene capacitors. The parasitic resistance losses of the impedance network inductors were calculated based on the measured inductor current and previously determined parasitic coil resistance, whereas the corresponding core losses were calculated according to the equation proposed by the core manufacturer [23].

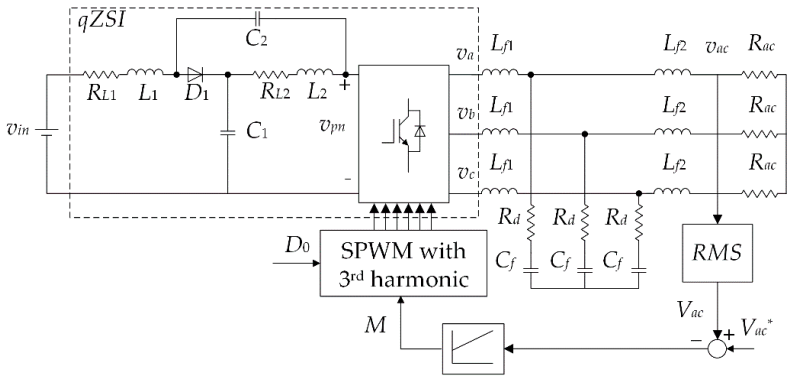


Figure 1. Control system of the qZSI in a stand-alone operation mode.

The semiconductor losses of the qZSI include the losses of the IGBTs, the FWDs, and the impedance network diode. The losses of the IGBTs include the conduction losses, the switching losses, and the

blocking losses. On the other hand, the losses of the diodes include the conduction losses, the reverse recovery losses, and the turn-on losses. The blocking losses of the IGBTs along with the turn-on losses of the diodes may be generally considered negligible. With respect to the above, two novel algorithms for calculation of the qZSI semiconductor losses are proposed in the next section.

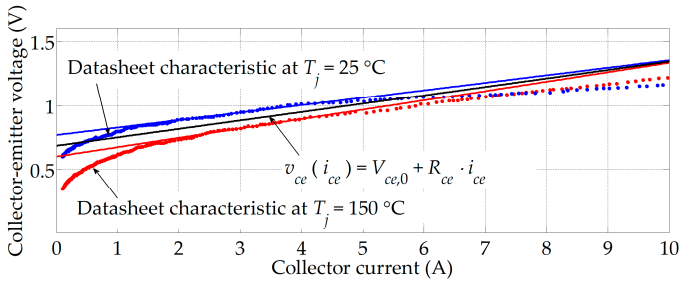
3. Proposed Semiconductor LCAs for the Quasi-Z-Source Inverter

In this section, two novel qZSI semiconductor LCAs are presented. Both the proposed LCAs calculate the losses of the IGBTs and FWDs in the three-phase inverter bridge and the losses of the impedance network diode. As for of the inverter bridge, the losses of a single upper IGBT-FWD pair were calculated and then multiplied by six in order to obtain the total bridge losses. The proposed LCAs require the output I–V characteristics of the IGBTs and diodes for calculation of the respective conduction losses, whereas the turn-on (only for the IGBT) and the turn-off characteristics are required for calculation of the respective switching losses. These characteristics are provided in the datasheet of the switching device manufacturer. Figure 2a shows the output I–V characteristics of the utilized IGBT. These characteristics have been linearized by considering the points taken from the datasheet graphs in the low-current range given the fact that the collector current in this study did not exceed 5 A. The IGBT threshold voltage (V_{ce0}) and the IGBT forward resistance (R_{ce}) were extracted for both provided junction temperatures (T_j = 25 °C and T_j = 150 °C). However, with the assumption that the actual junction temperature during normal operation is somewhere between these two values, final values of $V_{ce,0}$ and R_{ce} were obtained by averaging the values extracted for the two provided temperatures. The I–V characteristics of the FWD and the impedance network diode were approximated in the same way. Finally, the approximated I–V characteristics are defined as follows:

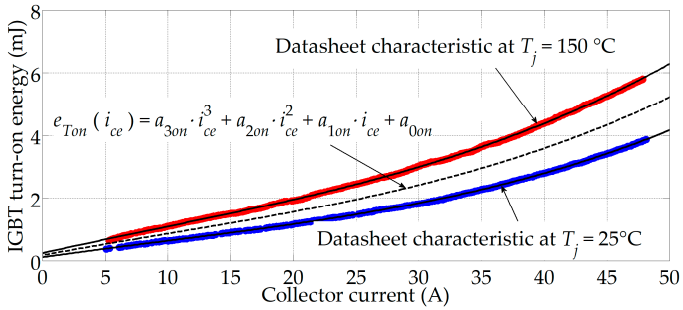
$$v_{ce}(i_{ce}) = V_{ce,0} + R_{ce} i_{ce} \tag{3}$$

$$v_{D/D1}(i_{D/D1}) = V_{D/D1,0} + R_{D/D1} i_{D/D1} \tag{4}$$

where v_{ce} and i_{ce} are the collector-emitter voltage and the collector current, respectively; $v_{D/D1}$, $V_{D/D1,0}$, $R_{D/D1}$, $i_{D/D1}$ are the forward voltage, the threshold voltage, the forward resistance, and the forward current of the FWD (subscript "*D*") and the impedance network diode (subscript "*D*1"), respectively.



(**a**)



(**b**)

Figure 2. I–V characteristics (**a**) and turn-on characteristics (**b**) of the utilized IGBT.

The values of the threshold voltage and the forward resistance for all the considered semiconductor devices are given in Appendix A.

The datasheets of all the semiconductor devices considered in this paper contain switching energy vs. current characteristics for the junction temperatures T_j = 25 °C and T_j = 150 °C. In addition, these characteristics are provided for the specified reference values of the inverter bridge input voltage (noted as V_{ref}) and the gate resistance. As an example, the IGBT turn-on energy (e_{Ton}) vs. the collector current is shown in Figure 2b. The characteristics were extracted for both the provided temperatures and approximated by utilizing the cubic fitting. The coefficients a_{0on}, a_{1on}, a_{2on}, a_{3on} (values given in Appendix A) were obtained by averaging the coefficients determined for the two provided temperatures. In this study, the actual inverter bridge input voltage was different from V_{ref}, so the calculated IGBT turn-on energy was scaled by the ratio $\left(V_{pn}/V_{ref}\right)^{k_T}$, according to the recommendations in [22,24], where k_T is the exponent representing the voltage dependence of the IGBT switching losses. On the other hand, the value of the gate resistance utilized in the experimental setup corresponded to the value given in the datasheet characteristics of interest. Finally, the same principle of the polynomial coefficient extraction has been applied for the IGBT turn-off characteristic and the reverse recovery characteristics of the qZSI diodes. Thus,

$$e_{Ton/off}(i_{ce}) = \left(\frac{V_{pn}}{V_{ref}}\right)^{k_T}\left(a_{3on/off}i_{ce}^3 + a_{2on/off}i_{ce}^2 + a_{1on/off}i_{ce} + a_{0on/off}\right) \tag{5}$$

$$e_{D/D1rr}(i_D) = \left(\frac{V_{pn}}{V_{ref}}\right)^{k_{D/D1}}\left(b_{3D/D1}i_{D/D1}^3 + b_{2D/D1}i_{D/D1}^2 + b_{1D/D1}i_{D/D1} + b_{0D/D1}\right) \tag{6}$$

where e_{Toff} is the turn-off switching energy of the IGBT; $e_{D/D1,rr}$ is the reverse recovery energy of the FWD (subscript "D") and the impedance network diode (subscript "$D1$"); $k_{D/D1}$ is the exponent representing the voltage dependence of the reverse recovery losses.

Values of the polynomial coefficients a_{off} and $b_{D/D1}$ are given in Appendix A, whereas V_{ref} of the considered IGBT and diodes is equal to 600 V. Finally, k_T = 1.4, $k_D = k_{D1}$ = 0.6 are chosen according to [24].

3.1. Loss-Calculation Algorithm 1

The first LCA is based on the methods which were in [11–13] used for the conventional VSI with the SPWM. However, in the considered qZSI configuration, the additional ST states occur, which make the loss calculation more complex.

The conduction losses of a single IGBT are calculated separately for the non-ST state and ST state. In both cases, the conduction losses are calculated based on the conduction energy. The phase current is assumed to be sinusoidal and the current ripple of the impedance network inductor is neglected. The IGBT conduction losses during the non-ST states ($P_{Tcond,nST}$) and the ST states ($P_{Tcond,ST}$) are, respectively, defined as follows (for more details see Appendix B, Equations (A1)–(A9)):

$$P_{Tcond,nST} = V_{ce,0}I_{phM}\left(\frac{1-D}{2\pi} + \frac{M\cos(\varphi)}{8}\right) + R_{ce}I_{phM}^2\left(\frac{1-D}{8} + \frac{M\cos(\varphi)}{3\pi} - \frac{M\cos(3\varphi)}{90\pi}\right) \tag{7}$$

$$P_{Tcond,ST} = D\left[R_{ce}\left(\frac{4}{9}I_L^2 + \frac{1}{8}I_{phM}^2\right) + V_{ce,0}\frac{2}{3}I_L\right] \tag{8}$$

where I_{phM} represents the phase current amplitude, I_L represents the mean value of the impedance network inductor current, φ represents the phase angle between the fundamental output phase current and voltage, and M represents the modulation index ($0 \le M \le 2/\sqrt{3}$).

The overall conduction losses of all the IGBTs in the three-phase inverter bridge are defined as follows:

$$P_{Tcond} = 6\left(P_{Tcond,nST} + P_{Tcond,ST}\right) \tag{9}$$

The conduction losses of the FWD are calculated based on its conduction energy. The overall conduction losses of all the FWDs (P_{Dcond}) in the three-phase inverter bridge are determined as follows (for more details see Appendix B, Equations (A10)–(A12)):

$$P_{Dcond} = 6\left[V_{D,0}I_{phM}\left(\frac{1-D}{2\pi} - \frac{M\cos(\varphi)}{8}\right) + R_D I_{phM}^2\left(\frac{1-D}{8} - \frac{M\cos(\varphi)}{3\pi} + \frac{M\cos(3\varphi)}{90\pi}\right)\right] \quad (10)$$

The impedance network diode conducts only during the non-ST states, whereby the diode current is assumed to be equal to I_L. The corresponding conduction losses are calculated based on the conduction energy. The conduction losses of the impedance network diode are calculated with the assumption that I_L is constant within a single T_{sw}, as follows (for more details see Appendix B, Equation (A13)):

$$P_{D1cond} = (1-D)\left(R_{D1}I_L^2 + V_{D1,0}I_L\right) \quad (11)$$

The switching losses of the IGBT consist of the switching losses of the non-ST states and the ST states. The switching losses of the non-ST states are caused by the switching transitions between the consecutive non-ST states. These losses may be calculated based on the total number of pulses N which occur within T.

$$\begin{aligned} P_{Ton,nST} &= \frac{1}{NT}\sum_n e_{Ton} \\ P_{Toff,nST} &= \frac{1}{NT}\sum_n e_{Toff} \end{aligned} \quad (12)$$

where $P_{Ton,nST}$ and $P_{Toff,nST}$ are the IGBT turn-on and turn-off losses during the switching transitions between the non-ST states, respectively.

The IGBT current is assumed to be sinusoidal during the non-ST states, which implies that the non-ST states switching losses are also sinusoidal. These losses occur only within the positive period of the phase current. By considering the facts mentioned above and switching frequency (f_{sw}), an approximation of Equation (12) can be given as follows:

$$\begin{aligned} P_{Ton,nST} &= \frac{1}{2\pi}\int_0^{\pi} f_{sw}e_{Ton}\left(I_{phM}\right)\sin(\omega t-\varphi)d\omega t = \frac{e_{Ton}\left(I_{phM}\right)}{\pi}f_{sw}\cos(\varphi) \\ P_{Toff,nST} &= \frac{1}{2\pi}\int_0^{\pi} f_{sw}e_{Toff}\left(I_{phM}\right)\sin(\omega t-\varphi)d\omega t = \frac{e_{Toff}\left(I_{phM}\right)}{\pi}f_{sw}\cos(\varphi) \end{aligned} \quad (13)$$

The switching losses of the ST states are caused by the switching transitions between the ST state and the non-ST state. The calculation of these losses is a bit more complex. The switching energies during these transitions are determined by the IGBT current during the ST state, which is equal to sum of 1/2 of the phase current and 2/3 of I_L. Accordingly, the ST state switching losses may be defined as follows:

$$\begin{aligned} P_{Ton,ST} &= \frac{f_{sw}}{2\pi}\int_0^{2\pi}\left[e_{Ton}\left(\tfrac{2}{3}I_L\right) + e_{Ton}\left(\frac{I_{phM}}{2}\right)\sin(\omega t-\varphi)\right]d\omega t \\ P_{Toff,ST} &= \frac{f_{sw}}{2\pi}\int_0^{2\pi}\left[e_{Toff}\left(\tfrac{2}{3}I_L\right) + e_{Toff}\left(\frac{I_{phM}}{2}\right)\sin(\omega t-\varphi)\right]d\omega t \end{aligned} \quad (14)$$

where $P_{Ton,ST}$ and $P_{Toff,ST}$ represent the ST states turn-on and turn-off switching losses, respectively.

The ST states switching losses depend on the number of the ST state turn-on and turn-off switching transitions that occur within one T_{sw}. However, during a single fundamental period of the phase current, this number is not constant. It varies depending on the sign of the phase current and the relation between the instantaneous values of the three reference voltages (v_{refA}, v_{refB}, v_{refC}). For example, the single period of the reference voltage (v_{refA}) is divided into five intervals, with each interval having a specific constant number of switching transitions within one T_{sw}. In the intervals where the corresponding phase current (i_{phA}) is negative, the IGBT conducts only during the ST states. Consequently, in these intervals, the ST state turn-on and turn-off switching transitions occur twice

within one T_{sw}. However, in the intervals where $i_{phA} > 0$, the number of the ST states switching transitions depends on the relation between v_{refA}, v_{refB}, and v_{refC}, due to the occurrence of the non-ST switching transitions at the intersection points of v_{refA} and the carrier triangular signal. The borders of these intervals are defined by the time points where v_{refA} intersects the remaining two reference voltages, and also by the time points of i_{phA} zero crossings.

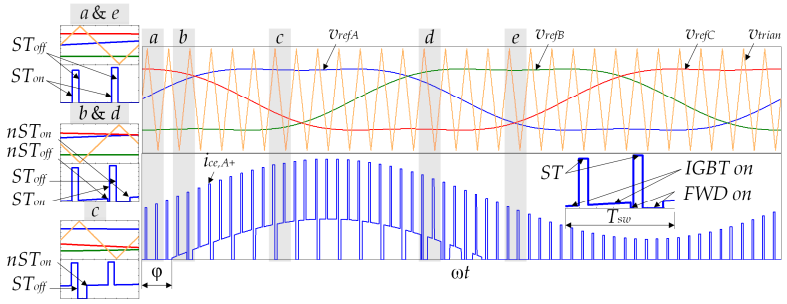
There are two separate set of equations for the calculation of the ST states switching losses. The first set applies for the phase angles between 0 and $\pi/6$ (case 1), whereas the second set applies for the phase angles between $\pi/6$ and $\pi/2$ (case 2). Tables 1 and 2 show the number of switching transitions in the defined intervals for the cases 1 and 2, respectively. The number of switching transitions given in the considered tables is defined based on Figure 3, where the period equal to ωT_{sw} is magnified within each considered phase angle interval. The labels a, b, c, d, e (a', b', c', d', e') represent only the part of the intervals I_1, I_2, I_3, I_4, I_5 (I'_1, I'_2, I'_3, I'_4, I'_5,), respectively, with the length equal to ωT_{sw}.

Table 1. The number of the switching transitions for the phase angle between 0 and $\pi/6$.

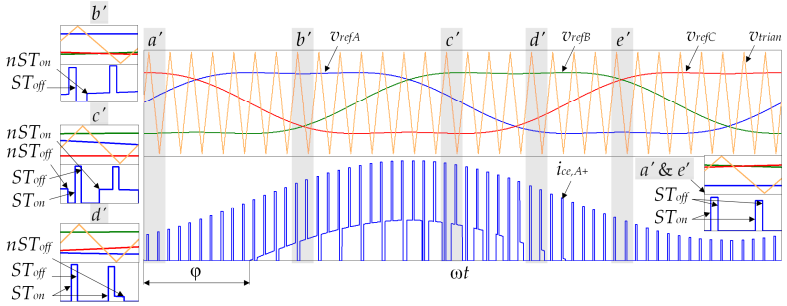
Interval	$N_{nST,on}$	$N_{nST,off}$	$N_{ST,on}$	$N_{ST,off}$
$I_1 = [0, \varphi]$	0	0	2	2
$I_2 = [\varphi, \pi/6]$	1	1	1	1
$I_3 = [\pi/6, 5\pi/6]$	1	0	0	1
$I_4 = [5\pi/6, (\pi + \varphi)]$	1	1	1	1
$I_5 = [(\pi + \varphi), 2\pi]$	0	0	2	2

Table 2. The number of the switching transitions for the phase angle between $\pi/6$ and $\pi/2$.

Interval	$N_{nST,on}$	$N_{nST,off}$	$N_{ST,on}$	$N_{ST,off}$
$I'_1 = [0, \varphi]$	0	0	2	2
$I'_2 = [\varphi, 5\pi/6]$	1	0	0	1
$I'_3 = [5\pi/6, 7\pi/6]$	1	1	1	1
$I'_4 = [7\pi/6, (\pi + \varphi)]$	0	1	2	1
$I'_5 = [(\pi + \varphi), 2\pi]$	0	0	2	2



(**a**)



(**b**)

Figure 3. Waveforms of the reference voltages, the carrier triangular signal, and the IGBT current for the phase angle between 0 and $\pi/6$ (**a**) and the phase angle between $\pi/6$ and $\pi/2$ (**b**).

In the case 1, shown in Figure 3a, the IGBT turns on straight into the ST state ($N_{ST,on}$) and turns off from the ST state ($N_{ST,off}$) twice during each T_{sw} in the intervals I_1 and I_5. In the intervals I_2 and I_4, both the ST switching transitions occur once during each T_{sw}, as well as the IGBT turn-on ($N_{nST,on}$) and turn-off ($N_{nST,off}$) transitions into non-ST states. On the other hand, in the interval I_3, the ST state occurs when the IGBT is already conducting, so there are no switching transitions ($N_{nST,off} = 0$ and $N_{ST,on} = 0$). Since the phase current is positive and the turn-off switching losses between non-ST states are already obtained from Equation (13), their influence has to be eliminated from the switching loss equations defined for the interval I_3. The ST states switching losses for the case 1 are calculated based on the number of switching transitions defined in Table 1 and Equation (14), as follows (for more details see Appendix C, Equation (A14)):

$$\begin{aligned} P_{Ton,ST} &= f_{sw}\left[\tfrac{7}{6}e_{Ton}\left(\tfrac{2}{3}I_L\right) - \tfrac{\sqrt{3}\cos(\varphi)+2}{2\pi}e_{Ton}\left(\tfrac{I_{phM}}{2}\right)\right] \\ P_{Toff,ST} &= f_{sw}\left[\tfrac{3}{2}e_{Toff}\left(\tfrac{2}{3}I_L\right) - \tfrac{1}{\pi}e_{Toff}\left(\tfrac{I_{phM}}{2}\right) - \tfrac{\sqrt{3}\cos(\varphi)}{2\pi}e_{Toff}\left(I_{phM}\right)\right] \end{aligned} \tag{15}$$

In the case 2, when φ is in between π/6 and π/2, the number of the switching transitions defined in Table 2 is determined based on Figure 3b. The ST states switching losses for the case 2 are calculated based on the number of switching transitions defined in Table 2 and Equation (14), as follows (for more details see Appendix C, Equation (A15)):

$$\begin{aligned} P_{Ton,ST} &= f_{sw}\left[\left(1+\tfrac{\varphi}{\pi}\right)e_{Ton}\left(\tfrac{2}{3}I_L\right) - \tfrac{\sqrt{3}\cos(\varphi)+2}{2\pi}e_{Ton}\left(\tfrac{I_{phM}}{2}\right) - e_{Ton}\left(I_{phM}\right)\tfrac{1-\cos(\varphi-\pi/6)}{2\pi}\right] \\ P_{Toff,ST} &= f_{sw}\left[\tfrac{3}{2}e_{Toff}\left(\tfrac{2}{3}I_L\right) - \tfrac{1}{\pi}e_{Toff}\left(\tfrac{I_{phM}}{2}\right) - \tfrac{\cos(\varphi+\pi/6)+1}{2\pi}e_{Toff}\left(I_{phM}\right)\right] \end{aligned} \tag{16}$$

The overall switching losses of the IGBTs in the three-phase inverter bridge are defined as follows:

$$P_{Tsw} = 6\left(P_{Ton,nST} + P_{Toff,nST} + P_{Ton,ST} + P_{Toff,ST}\right) \tag{17}$$

The FWD conducts only the phase current, so the reverse recovery losses of the diode are also sinusoidal. The overall reverse recovery losses of all six FWDs (P_{Drr}) in the three-phase inverter bridge are determined as follows:

$$P_{Drr} = 6\frac{f_{sw}}{2\pi}\int_0^{\pi} e_{Drr}\left(I_{phM}\right)\sin(\omega t-\varphi)d\omega t = 6\frac{f_{sw}}{2\pi}\int_0^{\pi} J d\omega t \tag{18}$$

The number of the reverse recovery switching transitions of the FWD is closely related to the IGBT turn-on switching transitions; namely, every time the IGBT turns on during the positive period of the phase current, the FWD recovers. That means that the total number of the diode reverse recoveries, in fact, equals the sum of the IGBT turn-on switching transitions ($N_{nST,on} + N_{ST,on}$) during the positive period of the phase current. Consequently, the reverse recovery losses of the FWDs have been calculated by considering the cases defined above. In case 1, based on Table 1 and Equation (18), P_{Drr} are defined as follows:

$$P_{Drr} = 6\frac{f_{sw}}{2\pi}\left[2\int_{\varphi}^{\frac{\pi}{6}} J d\omega t + \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} J d\omega t + 2\int_{\frac{5\pi}{6}}^{(\varphi+\pi)} J d\omega t\right] = 6f_{sw}\frac{4-\sqrt{3}\cos(\varphi)}{2\pi}e_{Drr}\left(I_{phM}\right) \tag{19}$$

In the case 2, based on Table 2 and Equation (18), P_{Drr} are defined as follows:

$$P_{Drr} = 6\frac{f_{sw}}{2\pi}\left[\int_{\varphi}^{\frac{5\pi}{6}} J d\omega t + 2\int_{\frac{5\pi}{6}}^{\frac{7\pi}{6}} J d\omega t + 2\int_{\frac{7\pi}{6}}^{(\varphi+\pi)} J d\omega t\right] = 6f_{sw}\frac{\sin(\varphi)-\sqrt{3}\cos(\varphi)+6}{4\pi}e_{Drr}\left(I_{phM}\right) \tag{20}$$

It is important to note that for the boundary phase angle of $\pi/6$, Equations (15) and (16) become equal, as well as Equations (19) and (20). Thus, the switching losses are changing continuously with the phase angle.

The impedance network diode recovers every time the ST state occurs, i.e., twice during each T_{sw}. With the reverse recovery current being considered equal to I_L, the reverse recovery losses of the impedance network diode are defined as follows:

$$P_{D1rr} = 2f_{sw}e_{D1rr}(I_L) \tag{21}$$

3.2. Loss-Calculation Algorithm 2

The second LCA is based on the algorithm presented in [20,21], which is for the first time here adapted for the qZSI. The corresponding flow chart is shown in Figure 4. The semiconductor losses are calculated by considering the instantaneous values of the following variables in kth and $(k-1)$st instants: the ST state signal (ST_{signal}), the non-ST state switching pulses of the IGBT (p), the phase current (i_{ph}), the impedance network diode current (i_{D1}), the impedance network inductor current (i_L), and the input voltage of the inverter (v_{in}).

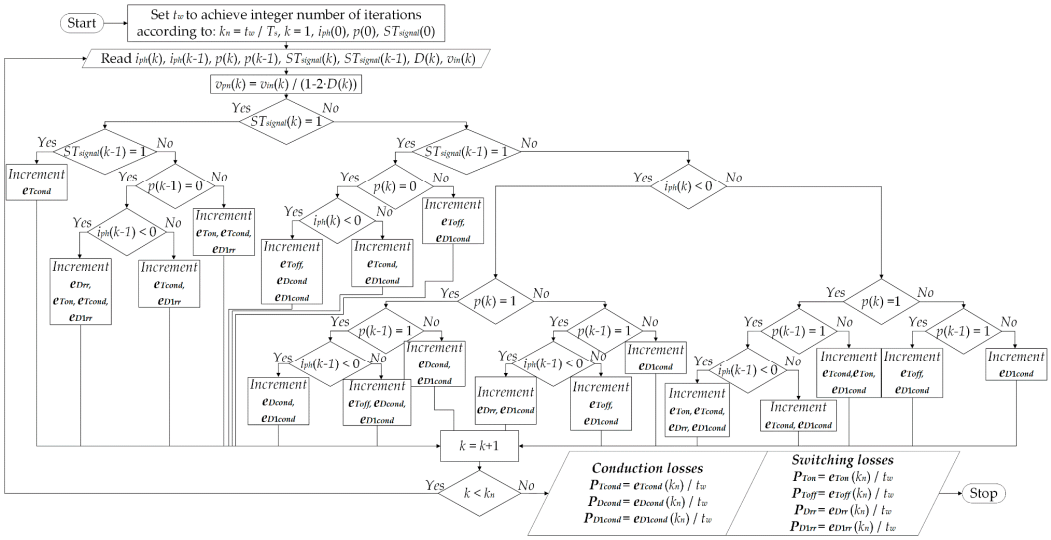


Figure 4. Flow chart of the LCA2.

The calculation of the IGBT conduction energy (e_{Tcond}) requires the value of the collector current. This current is equal to the phase current (i_{ph}) during the non-ST states. However, during the ST states, it is equal to the sum of one half of the phase current and two thirds of the impedance network inductor current. The IGBT conduction energy is calculated as follows:

$$\begin{aligned} e_{Tcond}(k) &= e_{Tcond}(k-1) + v_{ce}(k)\left|i_{ce}(k)\right|[t(k) - t(k-1)] \\ v_{ce}(k) &= V_{ce,0} + R_{ce}\left|i_{ce}(k)\right| \end{aligned} \tag{22}$$

The FWD does not conduct during the ST state, whereas it conducts part of the phase current during the negative half-period. The FWD conduction energy is defined as follows:

$$\begin{aligned} e_{Dcond}(k) &= e_{Dcond}(k-1) + v_D(k)\left|i_{ph}(k)\right|[t(k) - t(k-1)] \\ v_D(k) &= V_{D,0} + R_D\left|i_{ph}(k)\right| \end{aligned} \tag{23}$$

Further, the turn-on (e_{Ton}) and the turn-off (e_{Toff}) switching energies of the IGBT are calculated based on the collector current, whereas the reverse recovery energy (e_{Drr}) of the FWD is calculated based on the phase current as follows:

$$e_{Ton/off}(k) = e_{Ton/off}(k-1) + e_{Ton/off}\left(\left|i_{ce}(k)\right|\right) \tag{24}$$

$$e_{Drr}(k) = e_{Drr}(k-1) + e_{Drr}\left(\left|i_{ph}(k)\right|\right) \tag{25}$$

The conduction energy (e_{D1cond}) and reverse recovery energy (e_{D1rr}) of the impedance network diode are calculated as follows:

$$\begin{aligned} e_{D1cond}(k) &= e_{D1cond}(k-1) + v_{D1}(k)\left|i_{D1}(k)\right|[t(k) - t(k-1)] \\ v_{D1}(k) &= V_{D1,0} + R_{D1}\left|i_{D1}(k)\right| \\ e_{D1rr}(k) &= e_{D1rr}(k-1) + e_{D1rr}\left(\left|i_{D1}(k)\right|\right) \end{aligned} \tag{26}$$

Finally, the calculation of the corresponding power losses requires dividing of the energies accumulated in the time window (t_w), corresponding to the integer number of cycles of the phase current, with the time window duration in seconds.

4. Experimental Testing and Evaluation

The laboratory setup of the system shown in Figure 1 was built in order to test the proposed LCAs. The qZSI was supplied by the dc power supply Chroma 62050H-600S which provides voltages up to 600 V and currents up to 8.2 A. The three-phase inverter bridge is composed of six IGBTs with integrated FWDs IRG8P60N120KD (International Rectifier). The gate drivers SKHI 22B(R) (Semikron) were utilized to drive the IGBTs. The impedance network diode was built as a parallel compound of four FWDs of the IGBT-FWD pair IRG8P25N120KD (International Rectifier) since the impedance network current would be too excessive for a single diode of this type. The parameters of the inductors and capacitors in the impedance network along with the LCL filter parameters are given in Appendix D. The control algorithm was implemented by means of the MicroLabBox (dSpace) microcontroller and executed with the sampling frequency of 10 kHz. The reference RMS value and frequency of the fundamental load phase voltage were set to 230 V and 50 Hz, respectively. The ST signals were injected by a hardware circuit placed in between the digital outputs of the MicroLabBox and the signal inputs of the gate drivers.

4.1. Implementation Requirements of the Proposed Loss-Calculation Algorithms

Implementation requirements represent the important factor in the analysis of the proposed LCAs. They include the computational requirements, the number of required input variables and parameters, and the number of additional current/voltage sensors required to implement the desired LCA. The common input variables of the proposed algorithms are D, i_L, V_{in}, and i_{ph}. The additional input parameters of the LCA1 are M and φ, whereas in the case of the LCA2, the additional input signals are the i_{D1} waveform, the ST state signal, and the non-ST state switching pulses.

The value of the duty cycle required for the implementation of the LCA2 was obtained from the control algorithm. On the other hand, the currents required for the implementation of the LCA2 (i_L, i_{ph}, i_{D1}) were measured by means of the Hall-effect transducers IT 60-S (LEM). The input voltage of the qZSI, also required for the implementation of the LCA 2, has been measured by means of the Hall effect transducers CV 3–500 (LEM).

The waveforms of the three input currents (i_L, i_{ph}, i_{D1}) and the non-ST state switching pulses of the IGBT, required by the LCA2, were recorded by the oscilloscope MDO 3014 (Tektronix), which ensures sampling frequencies (f_{samp}) up to 10 MHz. The waveform of the qZSI input voltage was recorded by the oscilloscope SDS 1104X-E (Siglent), whereas the ST state signal was reconstructed based on the i_{D1} waveform, as shown in Figure 5. During the ST states ($ST_{signal} = 1$), i_{D1} is zero, whereas during the non-ST states ($ST_{signal} = 0$), this current is always positive.

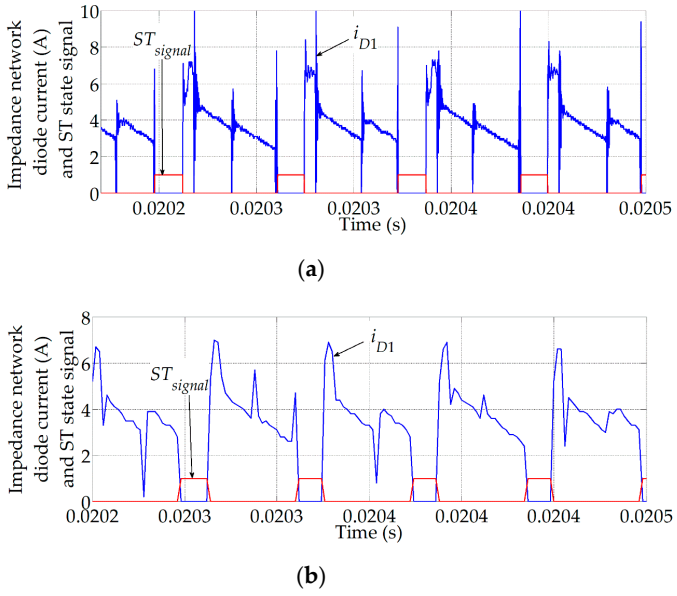


Figure 5. Waveforms of the impedance network diode current and the ST signal for the switching frequency of 8 kHz and sampling frequencies of 10 MHz (**a**) and 500 kHz (**b**).

The signals acquired by the oscilloscope MDO 3014 were originally sampled at 10 MHz and subsequently downsampled to determine the minimum value of f_{samp} that still allows capturing the required information from the recorded waveforms. With regard to this, the waveforms of i_{D1} and ST_{signal} were analyzed for the highest switching frequency considered in this study, which is 8 kHz. The minimum sufficient f_{samp} obtained for this case is also sufficient for switching frequencies lower than 8 kHz because lower f_{sw} implies lower minimum f_{samp}. During the measurement of the waveforms shown in Figure 5, the ST duty cycle was 0.22, which along with f_{sw} = 8 kHz, according to Equation (1), determines the ST state duration $T_0/2$ = 13.75 µs. For f_{samp} = 10 MHz (Figure 5a), the measured duration of each ST state ($T_0/2$) deviated by about ± 0.7 µs from the mentioned calculated value. This deviation is a consequence of an error induced by the hardware circuit that injects the ST signals. The goal was to retain approximately the same deviation of $T_0/2$ value while reducing f_{samp}. The minimum f_{samp} value for which this was achieved was equal to 500 kHz (Figure 5b). For the sampling frequencies lower than 500 kHz, the i_{D1} waveform could not be any more faithfully reconstructed, which led to an error in $T_0/2$ value of up to 3 µs.

The impedance network inductor current waveform shown in Figure 6 was also sampled with the frequency of f_{samp} = 500 kHz, although this signal could be faithfully reconstructed by applying the sampling frequency as low as 100 kHz. However, it is mandatory for the non-ST state switching pulses of the IGBT to be sampled with the same frequency as the waveform of i_{D1} in order to avoid the mismatch between that signal and the reconstructed ST state signal. Finally, the waveforms of the phase current and the qZSI input voltage were sampled with 10 kHz.

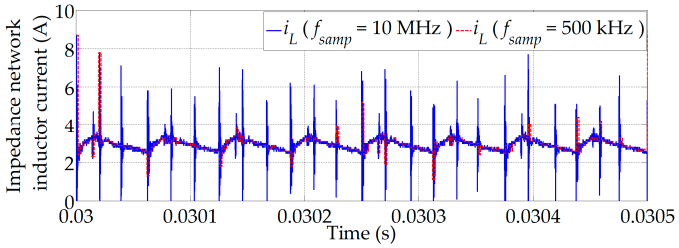


Figure 6. Waveform of the impedance network inductor current for the switching frequency of 8 kHz and sampling frequencies of 10 MHz and 500 kHz.

The LCA1 requires the values of M, D, φ, I_L, V_{in}, and I_{phM} for implementation. The latter three values may be relatively easily determined from the measured waveforms, whereas the values of M and D are obtained from the control algorithm. However, the value of φ has to be either determined from the measured phase current and voltage or known in advance (e.g., for a resistive load, $\varphi = 0$).

It may be concluded that the implementation of the LCA2 is more complex primarily due to an additional current sensor required for i_{D1}. Moreover, all three additional input signals required by the LCA2 have to be sampled with high sampling frequencies (i.e., 500 kHz or higher for the setup used in this study).

4.2. Experimental Results

All the experiments were carried out with the three-phase resistive load ($\varphi = 0$) connected to the inverter output. Figure 7 shows the semiconductor power losses distribution with respect to the switching frequency, RMS value of the phase current, qZSI input voltage, and duty cycle. During the variation of the switching frequency, the other system parameters were $D = 0.22$, $I_{ph} = 1.72$ A, $V_{in} = 450$ V, whereas the variation of I_{ph}, V_{in}, and D was carried out with the switching frequency set to 5 kHz. Different RMS values of the phase current were achieved by varying the load resistance, with $D = 0.22$ and $V_{in} = 450$ V. The variation of the input voltage was carried out with $D = 0.18$ and $I_{ph} = 1.72$ A, whereas the variation of the duty cycle was carried out with $V_{in} = 470$ V and $I_{ph} = 1.72$ A. The selected ranges of V_{in} and D were determined by considering several limitations of the utilized laboratory setup; namely, the combination of high input voltage and high ST duty cycle may result in IGBT collector-emitter voltage higher than the allowed maximum value of 1200 V, which may ultimately destroy the device. On the other hand, too low an input voltage would require a higher than allowed modulation index, whose value, according to the maximum constant boost strategy, must not exceed $2/\sqrt{3}(1-D)$ in order to maintain the six active states of the inverter intact [4]. Finally, high input voltage in combination with high duty cycle may cause the electromagnetic interference, which may disrupt the normal operation of the gate drivers.

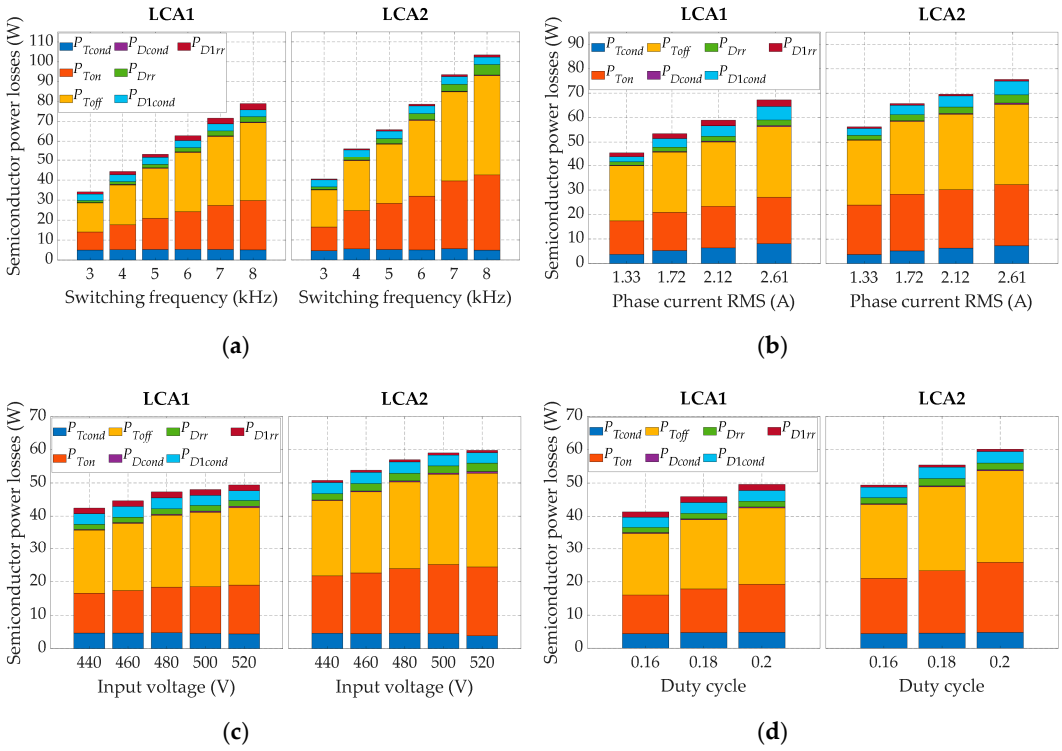


Figure 7. Semiconductor power losses distribution with respect to: switching frequency (**a**), RMS phase current (**b**), input voltage (**c**), and duty cycle (**d**).

The increase of the semiconductor losses with all four varied parameters was noted for both the proposed algorithms. However, arguably the largest increase is noted with the increase of the switching frequency. For example, at f_{sw} = 3 kHz, the total semiconductor losses calculated by the LCA1 and LCA2 amounted to P_{LCA1} = 34 W and P_{LCA2} = 40 W, respectively, whereas at f_{sw} = 8 kHz, these values have more than doubled and amounted to P_{LCA1} = 79 W and P_{LCA2} = 103 W, respectively. On the other hand, a less pronounced change in the semiconductor losses was noted in the considered ranges of the phase current, the input voltage, and the duty cycle.

Both algorithms indicate that the total losses of the IGBTs, considered as the sum of the respective switching and conduction losses, are dominant compared to the total diode losses and account for approximately 87% of the total semiconductor losses. In addition, the IGBT conduction losses account for approximately 10% of the total IGBT losses for both the algorithms. These losses are practically unaffected by the switching frequency and duty cycle since the IGBT current remains the same with the variation of these two parameters. However, the conduction losses increase with the phase current, whereas they decrease with the input voltage due to the decrease of the qZSI input current for the same applied load. The IGBT switching losses, which account for approximately 90% of the total IGBT losses, consist of the turn-on (P_{Ton}) and turn-off (P_{Toff}) switching losses. These losses significantly increase with the switching frequency due to the increase of the number of switching transitions. The same tendency is noted with the increase of the phase current due to the increase of switching energies according to Equation (5). The switching losses of the IGBTs also increase with the duty cycle and the input voltage due to the increase of V_{pn} as per Equation (2). The total losses of the FWDs account for approximately 5% of the total semiconductor losses, where the reverse recovery losses are dominant over the conduction losses. Finally, the remaining 8% of the total semiconductor losses belong to the impedance network diode losses, with the conduction losses being dominant over the reverse recovery losses. The mentioned losses of the qZSI's diodes have similar behavior as the losses of the IGBTs in terms of variation with f_{sw}, i_{ph}, V_{in}, and D.

The semiconductor losses calculated by the two proposed LCAs have been compared with the measured ones. For that purpose, the input and output inverter power along with the power losses of the impedance network inductors (P_L) and capacitors had to be obtained. As in [25], the copper losses of the impedance network inductors were calculated based on the respective current and the parasitic coil resistance. Likewise, the inductors' core losses were calculated according to the equation proposed in the datasheet of the core manufacturer [23]. The same datasheet shows that the losses of this core type are practically unaffected by the core temperature in the case of a continuous operation of up to 10 h, regardless of the values of the switching frequency and the magnetic induction. Since the experiments in this study lasted less than one hour, the temperature impact was neglected. The power losses of the impedance network capacitors were neglected due to the low ESR value. The inverter input power P_{in} was obtained as the mean value of $i_L \cdot v_{in}$, whereas the inverter output power (P_{acinv}) was measured by the high-precision power analyzer Norma 4000 (Fluke). The semiconductor losses were ultimately obtained as $P_{in} - P_{acinv} - P_L$, with the wire parasitic resistance losses considered negligible.

Figure 8 shows the comparison between the measured semiconductor losses ($P_{measured}$) and the calculated semiconductor losses from Figure 7. The absolute errors of both the LCA1 and LCA2 increase significantly with the switching frequency as shown in Table 3. On the other hand, the absolute errors of the proposed algorithms only slightly increase with the phase current RMS value, qZSI input voltage and duty cycle. Overall, the LCA2 provided more accurate results for all the considered values of f_{sw}, i_{ph}, V_{in}, and D. By assuming that the inductor core losses are calculated accurately, that the capacitor losses are negligible, and that both the input and output power of the inverter are accurately measured, the remaining differences between the measured and calculated losses are ascribed to the LCA errors. The errors of both the proposed LCAs significantly increase with the switching frequency. It is suspected that the values of the switching energies in the considered laboratory setup were higher than the values provided in the datasheet of the IGBT manufacturer, which are determined based on the double-pulse test. This is, presumably, due to the shortcomings of the double-pulse test such as

errors in the calculation of switching energies due to inaccuracies in voltage/current measurement or the influence of the parasitic capacitances and additional loop inductance/resistance within the test circuitry on the switching energies, as described in [26].

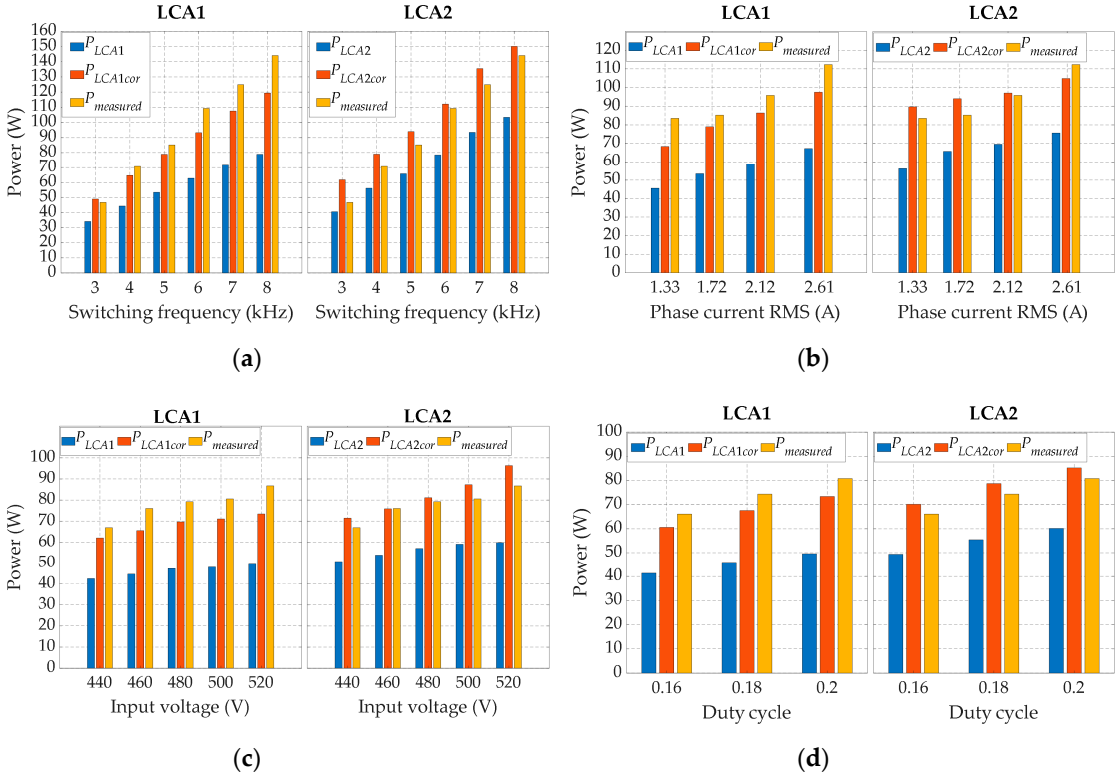


Figure 8. Measured and calculated semiconductor losses with respect to: switching frequency (**a**), RMS phase current (**b**), input voltage (**c**), and duty cycle (**d**).

Table 3. Absolute and relative errors with respect to the measured semiconductor losses of the proposed LCAs.

Switching Frequency	LCA1	LCA1cor	LCA2	LCA2cor
3 kHz	12 W (25%)	−2 W (−4%)	6 W (12%)	−15 W (−31%)
4 kHz	27 W (38%)	6 W (8%)	15 W (21%)	−8 W (−11%)
5 kHz	32 W (37%)	6 W (7%)	19 W (22%)	−9 W (−10%)
6 kHz	46 W (42%)	16 W (14%)	30 W (27%)	−3 W (−3%)
7 kHz	53 W (43%)	17 W (14%)	32 W (25%)	−10 W (−8%)
8 kHz	65 W (45%)	24 W (16%)	40 W (27%)	−6 W (−4%)

The influence of the switching frequency on the switching losses may be shown by considering the temperature of the semiconductor device. For that purpose, the IGBT-FWD case temperature was measured in steady state by means of the thermal camera Testo 865 (Testo) for all the considered switching frequencies. Figure 9 shows that, for the frequency increase from 3 kHz to 7 kHz, the IGBT-PWD case temperature increased by a total of 11 °C. However, when the switching frequency was increased from 7 kHz to 8 kHz, the temperature increased for 12 °C. These results confirm that the IGBT-FWD switching losses significantly increase with the switching frequency since the conduction losses are not affected by the switching frequency. The temperature increase is presumably caused by the increase of the IGBT switching losses, since both the proposed algorithms indicate that they are dominant over the FWD switching losses.

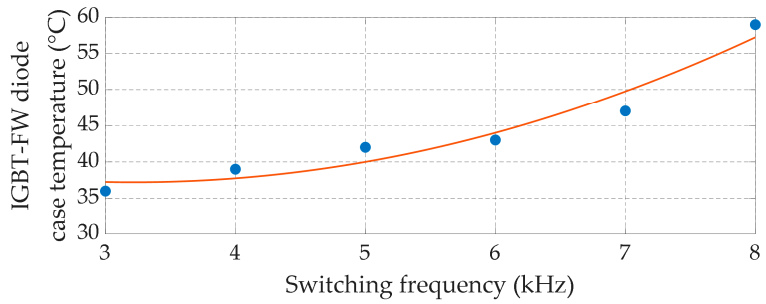


Figure 9. Measured temperature of the IGBT-FWD case at different switching frequencies.

4.2.1. Correction of the IGBT Switching Losses Calculation

As a way of simple correction of the calculated IGBT switching losses, the IGBT turn-on and turn-off switching energies defined in Equation (5) were multiplied by the same factor greater than 1 with the aim of reducing the LCA2 error to zero. The LCA2 was chosen for the correction because it involves far less simplifications compared to the LCA1 so it, expectedly, provided more accurate results prior to the correction. The final value of the multiplication factor was determined by averaging the values obtained for several measurement points. For that purpose, four points with the I_{ph} values of 1.33 A, 1.72 A, 2.12 A, and 2.61 A were chosen. For all the considered points, the switching frequency was set to 5 kHz and V_{pn} amounted to 800 V, thus maintaining the constant V_{pn}/V_{ref} ratio. Hence, the influence of k_T was the same for all the considered measurement points. The value of the average multiplication factor obtained in this manner is 1.53, which implies 53% higher IGBT switching energies. Note that by applying the multiplication factor in the described manner, all the other remaining errors, such as the input/output power measurement errors, are ascribed as the calculation error of the IGBT switching losses. Ultimately, the same value of the corrective multiplication factor was applied for both the LCAs.

Figure 8 shows the comparison between the proposed LCAs-prior and after the correction of the IGBT switching energies- and the measured semiconductor losses. In Table 3, the absolute and relative errors are given with respect to the measured semiconductor losses for all the considered f_{sw} values. The accuracy of the LCAs notably increased after the correction of the IGBT switching energies. The same tendency is noted with regard to the qZSI input voltage, the phase current, and the duty cycle.

4.2.2. Efficiency and Semiconductor Losses Share of the qZSI

Figure 10 shows the qZSI efficiency and the share of the measured semiconductor losses in the total inverter losses with respect to the switching frequency. The inverter efficiency decreases approximately linearly in the considered frequency interval, whereas the share of the measured semiconductor losses increases rapidly from about 50% at f_{sw} = 3 kHz to almost 85% at f_{sw} = 8 kHz.

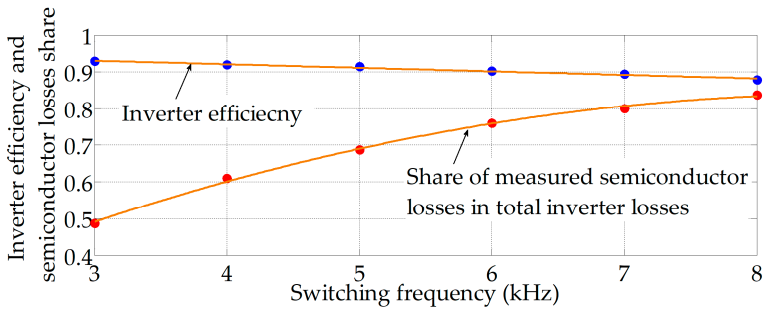


Figure 10. Inverter efficiency and share of measured semiconductor losses in total inverter losses with respect to switching frequency.

5. Conclusions

This paper presents two novel semiconductor LCAs for the three-phase qZSI. The proposed LCAs were successfully applied for the considered inverter in the stand-alone operation mode. However, the proposed algorithms are also applicable for different control systems as well as for grid-tied applications. Both the proposed LCAs indicate that the losses of the transistors are dominant and account for approximately 87% of all the semiconductor losses. Of all transistor losses, the switching losses are dominant with the percentage of 90%. The differences noted between the measured and calculated semiconductor losses are, presumably, due to the differences between the actual switching energies and those provided in the datasheet of the transistor manufacturer. Therefore, the transistor datasheet switching energies, which were used as the input data for the LCAs, were multiplied by the experimentally determined factor of 1.53, which resulted in the mean absolute percentage errors of 11.2% and 7.9% for the LCA1 and LCA2, respectively. Alternatively, instead of relying on the manufacturers characteristics, more accurate IGBT switching characteristics may be obtained prior to LCAs implementation (e.g., determined experimentally from the measurements taken in the normal operating conditions of the considered qZSI) and then used as the input data for the LCAs, and even scaled with respect to the actual measured IGBT case temperature. The experimental results indicate that the qZSI semiconductor losses significantly drop with the switching frequency, resulting in better inverter efficiency. On the other hand, the total harmonic distortion value of the phase currents increases at lower switching frequencies, thus making filter design a more demanding task.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Polynomial coefficients in Equations (3)–(6)

$R_{ce} = 0.066105\ \Omega$, $V_{ce,0} = 0.6823$ V
$R_D = 0.0862\ \Omega$, $V_{D,0} = 0.774$ V
$R_{D1} = 0.1225\ \Omega$, $V_{D1,0} = 0.999$ V
$a_{0on} = 0.18$, $a_{1on} = 0.074$, $a_{2on} = -7.2 \times 10^{-4}$, $a_{3on} = 2.537 \times 10^{-5}$
$a_{0off} = 0.258$, $a_{1off} = 0.081$, $a_{2off} = -1.41 \times 10^{-4}$, $a_{3off} = 0$
$b_{0D} = 0.036$, $b_{1D} = 0.04$, $b_{2D} = -3.76 \times 10^{-4}$, $b_{3D} = 9.9 \times 10^{-7}$
$b_{0D1} = 0.0145$, $b_{1D1} = 0.052$, $b_{2D1} = -0.0012$, $b_{3D1} = 5.34 \times 10^{-6}$

Appendix B

The conduction energy of the IGBT during the non-ST states within one T_{sw} are given by

$$E_{Tcond,nST} = v_{ce} i_{ce,nST} d_{T,nST} T_{sw} \tag{A1}$$

where $i_{ce,nST} = I_{phM} \sin(\omega t)$, $d_{T,nST}$ represents the IGBT duty cycle during the non-ST states, which is, in turn, defined as follows:

$$d_{T,nST} = \frac{1}{2}\left\{1 + M\left[\sin(\omega t + \varphi) + \frac{1}{6}\sin[3(\omega t + \varphi)]\right]\right\} - \frac{D}{2} \tag{A2}$$

The first term in Equation (A2) represents the duty cycle in the case when the traditional SPWM with the injected 3rd harmonic is implemented. The factor –D/2 appears in Equation (A2) in order to

eliminate the impact of the corresponding ST state (Figure 3a, lower right corner). By substituting Equations (3) and (A2) in Equation (A1), it becomes

$$E_{Tcond,nST} = \left(R_{ce}I_{phM}\sin(\omega t) + V_{ce0}\right)I_{phM}\sin(\omega t)\left\{\frac{1}{2}\left\{1 + M\left[\sin(\omega t + \varphi) + \frac{1}{6}\sin[3(\omega t + \varphi)]\right]\right\} - \frac{D}{2}\right\}T_{sw} \quad \text{(A3)}$$

Based on the differential form of Equation (A3) ($T_{sw} = dt = T/2\pi\, d\omega t$), the IGBT conduction losses that occur during the non-ST states are defined as follows:

$$P_{Tcond,nST} = \frac{1}{T}\int_0^{T/2} dE_{Tcond,nST} = \frac{1}{2\pi}\int_0^{\pi} E_{Tcond,nST}\, d\omega t \quad \text{(A4)}$$

By substituting Equation (A3) into Equation (A4), $P_{Tcond,nST}$ are defined as follows:

$$P_{Tcond,nST} = \frac{I_{phM}}{4\pi}\int_0^{\pi}\left(R_{ce}I_{phM}\sin(\omega t) + V_{ce,0}\right)\sin(\omega t)\left\{1 - D + M\left[\sin(\omega t + \varphi) + \frac{1}{6}\sin[3(\omega t + \varphi)]\right]\right\} d\omega t \quad \text{(A5)}$$

The final expression of $P_{Tcond,nST}$ is obtained by solving the integral on the right-hand side of Equation (A5).

The conduction energy of the IGBT during the ST states within one T_{sw} is given by

$$E_{Tcond,ST} = v_{ce}i_{ce,ST}DT_{sw} \quad \text{(A6)}$$

The IGBT current during the ST state may be approximated as follows [14]:

$$i_{ce,ST} = \frac{2}{3}I_L + \frac{1}{2}I_{phM}\sin(\omega t) \quad \text{(A7)}$$

By substituting Equations (3) and (A7) in Equation (A6), it becomes

$$E_{Tcond,ST} = \left[R_{ce}\left(\frac{2}{3}I_L + \frac{1}{2}I_{phM}\sin(\omega t)\right) + V_{ce,0}\right]\left(\frac{2}{3}I_L + \frac{1}{2}I_{phM}\sin(\omega t)\right)DT_{sw} \quad \text{(A8)}$$

Based on the differential form of Equation (A8) ($T_{sw} = dt = T/2\pi\, d\omega t$), the IGBT conduction losses that occur during the ST states are defined as follows:

$$P_{Tcond,ST} = \frac{1}{2\pi}\int_0^{2\pi}\left[R_{ce}\left(\frac{2}{3}I_L + \frac{1}{2}I_{phM}\sin(\omega t)\right) + V_{ce,0}\right]\left(\frac{2}{3}I_L + \frac{1}{2}I_{phM}\sin(\omega t)\right)Dd\omega t \quad \text{(A9)}$$

The final expression of $P_{Tcond,ST}$ is obtained by solving the integral on the right-hand side of Equation (A9).

The conduction energy of the FWD within one T_{sw} is defined as follows:

$$E_{Dcond} = i_{ce,nST}v_D(1 - d_{T,nST} - D)T_{sw} = v_D d_D T_{sw} i_{ce,nST} \quad \text{(A10)}$$

where the FWD current is assumed to be sinusoidal, whereas the diode duty cycle (d_D) is defined according to the $d_{T,nST}$ and D, as follows:

$$d_D = \frac{1}{2}\left\{1 - M\left[\sin(\omega t + \varphi) + \frac{1}{6}\sin[3(\omega t + \varphi)]\right]\right\} - \frac{D}{2} \quad \text{(A11)}$$

By substituting Equations (4) and (A11) into Equation (A10), it becomes

$$E_{Dcond} = \left(R_D I_{phM} \sin(\omega t) + V_{D,0}\right) I_{phM} \sin(\omega t) \left\{ \frac{1}{2} \left\{ 1 - M \left[\sin(\omega t + \varphi) + \frac{1}{6} \sin[3(\omega t + \varphi)] \right] \right\} - \frac{D}{2} \right\} T_{sw} \quad \text{(A12)}$$

The FWD conduction losses (P_{Dcond}) were calculated as the integral of the differential form of Equation (A12), similarly as the IGBT conduction losses.

The impedance network diode conduction energy within one T_{sw} is defined as follows:

$$E_{D1cond} = (R_{D1} I_L + V_{D1,0}) I_L (1 - D) T_{sw} \quad \text{(A13)}$$

Appendix C

Calculation of the switching losses in LCA1 for $0 < \varphi < \pi/6$

$$\begin{aligned} P_{Ton,ST} &= \frac{f_{sw}}{2\pi} \left[2 \int_0^{\varphi} K d\omega t + \int_{\varphi}^{\frac{\pi}{6}} K d\omega t + \int_{\frac{5\pi}{6}}^{(\pi+\varphi)} K d\omega t + 2 \int_{(\pi+\varphi)}^{2\pi} K d\omega t \right] \\ P_{Toff,ST} &= \frac{f_{sw}}{2\pi} \left[2 \int_0^{\varphi} I d\omega t + \int_{\varphi}^{\frac{\pi}{6}} I d\omega t + \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} I d\omega t + \int_{\frac{5\pi}{6}}^{(\pi+\varphi)} I d\omega t + 2 \int_{(\pi+\varphi)}^{2\pi} I d\omega t - \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} e_{off}\left(I_{phM}\right) \sin(\omega t - \varphi) d\omega t \right] \end{aligned} \quad \text{(A14)}$$

Calculation of the switching losses in LCA1 for $\pi/6 < \varphi < \pi/2$

$$\begin{aligned} P_{Ton,ST} &= \frac{f_{sw}}{2\pi} \left[2 \int_0^{\varphi} K d\omega t + \int_{\frac{5\pi}{6}}^{\frac{7\pi}{6}} K d\omega t + 2 \int_{\frac{7\pi}{6}}^{(\pi+\varphi)} K d\omega t + 2 \int_{(\pi+\varphi)}^{2\pi} K d\omega t - \int_{\frac{7\pi}{6}}^{(\pi+\varphi)} e_{Ton}\left(I_{phM}\right) \sin(\omega t - \varphi) d\omega t \right] \\ P_{Toff,ST} &= \frac{f_{sw}}{2\pi} \left[2 \int_0^{\varphi} I d\omega t + \int_{\varphi}^{\frac{5\pi}{6}} I d\omega t + \int_{\frac{5\pi}{6}}^{\frac{7\pi}{6}} I d\omega t + \int_{\frac{7\pi}{6}}^{(\pi+\varphi)} I d\omega t + 2 \int_{(\pi+\varphi)}^{2\pi} I d\omega t - \int_{\varphi}^{\frac{5\pi}{6}} e_{Toff}\left(I_{phM}\right) \sin(\omega t - \varphi) d\omega t \right] \end{aligned} \quad \text{(A15)}$$

where $K = e_{Ton}\,(2/3I_L) + e_{Ton}\,(I_{phM}/2)\,\sin(\omega t - \varphi)$, $I = e_{Toff}\,(2/3I_L) + e_{Toff}\,(I_{phM}/2)\,\sin(\omega t - \varphi)$

Appendix D

Parameters of the impedance network inductors:
T520-26 powder cores (Micrometals), L = 20.2 mH (unsaturated), and R_L = 0.5 Ω (at 25 °C).
Parameters of the impedance network capacitors:
MKSPI35-50U/1000 polypropylene capacitors (Miflex), C = 50 µF, and ESR = 7.8 mΩ.
Parameters of the output LCL filter:
L_{f1} = 8.64 mH, L_{f2} = 4.32 mH, C_f = 4 µF, and R_d = 10 Ω.

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Znanstveni rad IV

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Efficiency Boost of a Quasi-Z-Source Inverter: A Novel Shoot-Through Injection Method with Dead-Time

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Abstract: A quasi-Z-source inverter (qZSI) is a single-stage inverter that enables a boost of the input dc voltage through the utilization of a so-called shoot-through state (STS). Generally, the efficiency of the qZSI depends on the utilized STS injection method to a significant extent. This paper presents a novel method of STS injection, called the zero-sync method, in which the STS occurrence is synchronized with the beginning of the zero switching states (ZSSs) of the three-phase sinusoidal pulse width modulation (SPWM). In this way, compared to the conventional STS injection method, the total number of switchings per transistor is reduced. The ZSSs are detected by utilizing the SPWM pulses and the logic OR gates. The desired duration of the STS is implemented by utilizing the LM555CN timer. The laboratory setup of the three-phase qZSI in the stand-alone operation mode was built to compare the proposed zero-sync method with the conventional STS injection method. The comparison was carried out for different values of the switching frequency, input voltage, duty ratio, and load power. As a result of the implementation of the zero-sync method, the qZSI efficiency was increased by up to 4%. In addition, the unintended STSs, caused by the non-ideal switching dynamics of the involved transistors, were successfully eliminated by introducing the optimal dead-time as part of the modified zero-sync method. As a result, the efficiency was increased by up to 12% with regard to the conventional method.

Keywords: dead-time; efficiency; hardware implementation; shoot-through injection; sinusoidal pulse width modulation; quasi-Z-source inverter

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1. Introduction

The Z-source inverter (ZSI), proposed in 2003, is a single-stage inverter with boost capability [1]. The essential part of the ZSI is an impedance network placed at the dc side of the inverter bridge and composed of two capacitors, two inductors, and a diode. The impedance network combined with the additional shoot-through switching state (STS) enables the boost of the input dc voltage. The STS is achieved by short circuiting one or all the inverter legs during the zero switching states (ZSSs) of the utilized pulse width modulation (PWM) scheme. Many modifications and improvements have been proposed for the ZSI topology [2–4], with the quasi-ZSI (qZSI) topology being one of the most commonly used [5]. The main advantages of the qZSI are continuous input current and reduced voltage rating of one of the capacitors in the impedance network. This is achieved through different arrangement of the components in the impedance network.

The commonly utilized sinusoidal PWM (SPWM) and the space-vector PWM (SVPWM) require modifications to allow the STS injection. In [6], the most common qZSI-compatible SVPWM methods are presented. They differ by the number of the STS occurrences within a single switching period, ranging from two to six. There are also many modifications of the SVPWM method which aim to improve the performance of different ZSI topologies. For example, the main goal of the method proposed in [7] was to reduce the switching losses, whereas in [8] the main goal was to reduce the common-mode voltage. The main

advantage of the SVPWM with regard to the SPWM is the higher achievable ac voltage at the inverter bridge output for a given input dc voltage. However, this disadvantage of the SPWM may be overcome by injecting 1/6 of the 3rd harmonic component into the respective reference signals [9]. Among the SPWM-based methods most commonly applied for the ZSI topologies are the simple-boost control (SBC), the maximum boost control (MBC) [10], and the maximum constant boost control (MCBC) [11,12]. All the mentioned methods imply that the value of the STS duty ratio (D_0), which is defined by the duration of the STS and the switching period, cannot be varied independently of the amplitude modulation index (M_a). This represents a significant disadvantage in terms of the control of the ZSI-related inverters in certain applications [13–17]. Therefore, the methods utilized in [13–17] allow D_0 value to vary regardless of the M_a value as long as D_0 value is lower than the maximum allowed, which is, in turn, defined by the applied M_a [11]. However, in the literature, the start of the STS is typically not synchronized with the start of the ZSS, except for the case of the MBC method. This results in additional ZSSs with respect to the case when the STS and ZSS would start simultaneously, leading to additional switching losses. In the conventional approach, utilized in [15,16], the STS signal is generated based on the comparison of two dc reference signals (positive and negative) with the carrier signal. However, in this case, the start of the STS is not synchronized with the start of the ZSS.

The STS injection into standard PWM schemes sometimes requires modifications in terms of the utilized hardware [18–22]. The STS implies short circuiting of the inverter phase legs, which is forbidden in the conventional voltage-source inverters (VSI) because it leads to the dc-link short circuit and, ultimately, to the inverter failure. Therefore, some microcontrollers, such as the MicroLabBox (dSpace) utilized in [18] and in this paper, do not allow the implementation of the STSs in the dedicated PWM blocks. One of the solutions is the introduction of the additional circuitry, as in [18–22], composed of the logic OR gates. Another is to impose the STSs by utilizing two different reference signals for the PWM pulses generation of two transistors from the same inverter leg [23,24]. However, the latter implies a high current ripple rating (approximately 130% of the mean value) of the impedance network inductors [23].

The conventional VSIs require the introduction of dead-time into the SPWM pulses in order to prevent short circuiting during the SPWM switching transitions, caused by the non-ideal switching of the involved transistors [25]. On the other hand, in the case of ZSI topologies, the introduction of the dead-time is not necessary due to the existence of the impedance network on the dc side of the inverter bridge [26,27]. However, by omitting the dead-time, a sporadic, unintended short circuiting is bound to occur across the inverter legs due to the aforementioned reason (as would be the case in the conventional VSIs if the dead-time was not introduced). Although these states would not cause the ZSI failure, they would result in an additional, unintended voltage boost. This phenomenon is more prominent at higher values of the inverter bridge input voltage due to the longer duration of the PWM switching transitions. To our best knowledge, in terms of ZSI-related topologies, only in [28] the dead-time was implemented in order to prevent unintended short circuiting across the inverter legs of the multi-level ZSI. In this case, the implementation of the dead-time caused the increase of a common-mode voltage which was reduced by means of the proposed SVPWM scheme. The reason for omitting the dead-time in the literature may be the fact that the peak value of the input voltage (with neglected overshoot) of an inverter bridge utilized in [1,5,7,8,10,12–17,19–22] was relatively low (approximately 500 V), so this phenomenon was not that prominent.

This paper presents a novel method of the STS injection into the three-phase SPWM and it is organized as follows. In Section 2, the basic theoretical background of the qZSI is provided. Section 3 presents the novel STS injection method, called the zero-sync method, in which the starts of the STSs and the ZSSs are synchronized. In this way, compared to the conventional STS injection method, the total number of switchings in the inverter bridge within a single period of the sinusoidal reference signal is reduced by approximately

four times the frequency modulation index (M_f). In Section 4, the additional circuitry required for the implementation of the zero-sync method is described. This circuitry detects the ZSS from the input SPWM pulses generated by a microcontroller and injects the STS pulses of adjustable, predefined duration into the SPWM pulses. In Section 5, a comparison of the zero-sync method and the conventional STS injection method is carried out by utilizing the laboratory setup of the three-phase qZSI in the stand-alone mode. The comparison is carried out for six values of the switching frequency from 5 kHz to 10 kHz and three values of the load power from 1000 W to 3000 W. The peak value of the voltage across the inverter bridge (with neglected transient overshoot) is varied in the range of 500–1200 V. In Section 6, the minimal necessary dead-time is additionally introduced to prevent unintended short circuiting across the inverter legs caused by the non-ideal switching of the involved transistors and, hence, to avoid the additional, uncontrollable voltage boost. Finally, in Section 7, the experimental results are discussed, whereas in Section 8 the conclusions are presented.

2. Quasi-Z-Source Inverter

The considered qZSI in the stand-alone configuration is shown in Figure 1. The main parts of the qZSI are the three-phase inverter bridge and the impedance network. The three-phase inverter bridge consists of the insulate gate bipolar transistors (IGBTs) with integrated free-wheeling diodes (FWDs). This paper considers a symmetrical impedance network, i.e., $L_1 = L_2 = L$, $C_1 = C_2 = C$. The additional LCL filter, composed of the inductors (L_{f1}, L_{f2}), capacitors (C_f), and dumping resistances (R_d), is connected at the inverter output. The SPWM with injected 3rd harmonic has been implemented, where the qZSI utilizes the standard SPWM switching states (also known as the non-STSs) along with the STSs, which are injected within the ZSSs. During the STSs, all the transistors in the three-phase inverter bridge conduct, leading to the input voltage boost

$$B = \frac{1}{1-2D_0} = \frac{1}{1-2\frac{T_0}{T_{sw}}} \tag{1}$$

where T_0 is the STS period and T_{sw} is the switching period.

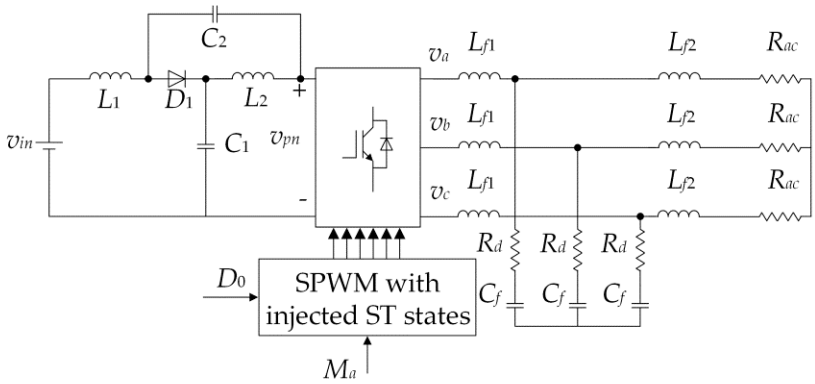


Figure 1. qZSI in a stand-alone configuration.

The peak value of the inverter bridge input voltage (V_{pn}) and the mean value of the voltages across the capacitors C_1 and C_2 (V_{C1} and V_{C2}) for the case of neglected parasitic voltage drops in the impedance network may be defined as follows:

$$\begin{aligned} V_{pn} &= BV_{in} = \tfrac{V_{in}}{1-2D_0} \\ V_{C1} &= V_{in}\tfrac{1-D_0}{1-2D_0} \\ V_{C2} &= V_{in}\tfrac{D_0}{1-2D_0} \end{aligned} \tag{2}$$

where V_{in} is the mean value of the qZSI input voltage.

3. Analysis of a Zero-Sync Shoot-Through State Injection Method

The main features of the zero-sync method are the injection of the STS right at the beginning of each ZSS and the control of the STS duration by means of the timer. The value of the maximum allowed STS duty ratio ($D_{0,max}$) is selected to be the same as for the maximum constant boost control (MCBC) with injected 3rd harmonic, as follows [11]:

$$D_{0,max} = 1 - \sqrt{3}/2M_a \quad (3)$$

This ensures that the STS lasts equal or less than the ZSS, while achieving a time-invariant boost of the inverter, corresponding to the applied D_0 value in the range $0 < D_0 < D_{0,max}$. The best way to describe the zero-sync method is by considering the corresponding waveforms. Figure 2a shows the waveforms of the reference voltages (v_{refA}, v_{refB}, v_{refC}), the carrier triangular signal (v_{trian}), the STS signal (ST_{tim}), and the SPWM pulses of all the transistors (S_{A+}, S_{A-}, S_{B+}, S_{B-}, S_{C+}, S_{C-}), with $0 < D_0 < D_{0,max}$. The STSs occur right at the beginning of each ZSS (denoted by dashed lines). During the STSs, the pulses of all the transistors are set to 1, which means that they all conduct.

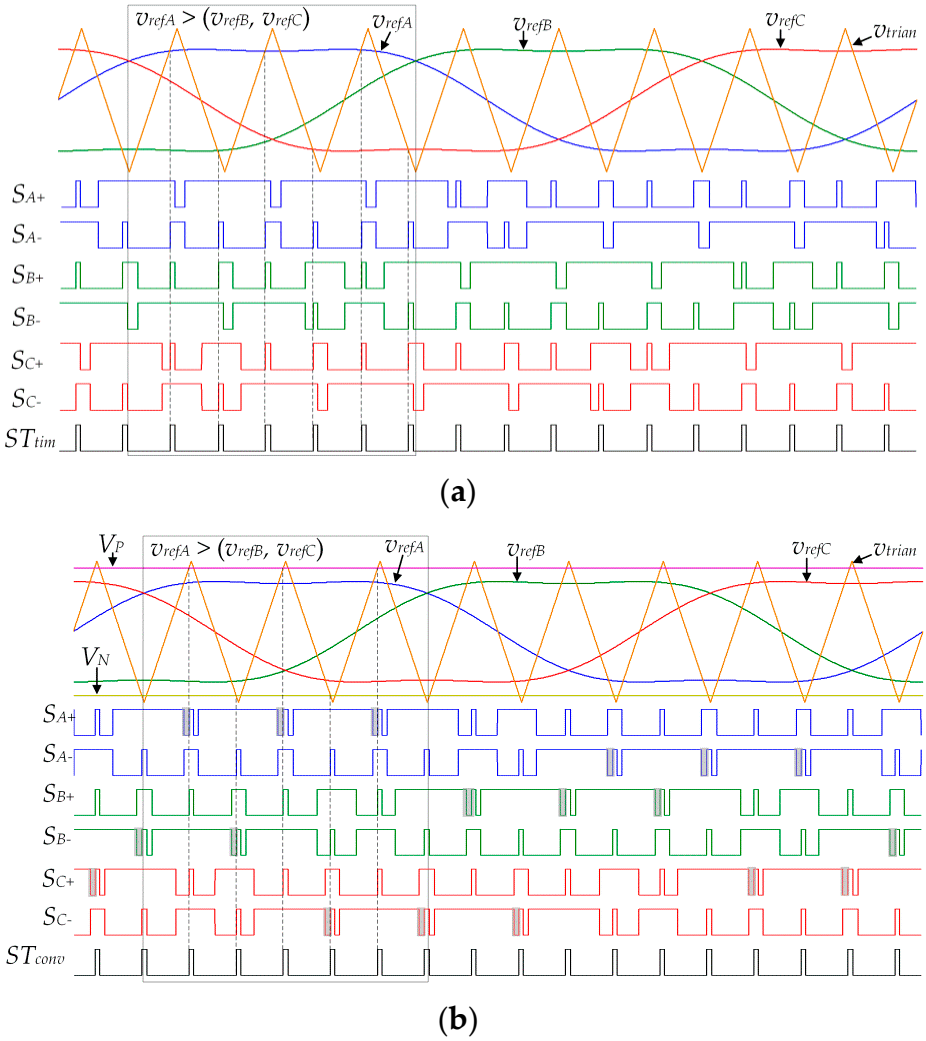


Figure 2. Waveforms of the zero-sync STS injection method (**a**) and the conventional STS injection method (**b**), with $0 < D_0 < D_{0,max}$.

The STS injection method considered in Figure 2b is the conventional method [15,16]. In this method, the STS signal (ST_{conv}) is obtained as a result of comparison of the reference dc voltages V_P and V_N with v_{trian}. The ST_{conv} value is equal to 1 in the case when $v_{trian} > V_P$ or $v_{trian} < V_N$, otherwise it is equal to 0.

There are notable differences in the switching states distribution between the two STSs injection methods shown in Figure 2, although the same values of M_a and D_0 were applied for both the methods. This phenomenon is analyzed for the corresponding transistor pulses of the phase A, where the same conclusion may be reached by considering the other two phases. The differences exist in the upper transistor pulse (S_{A+}) during the interval where the instantaneous value of v_{refA} is higher than the values of v_{refB} and v_{refC}. In that interval, the switching states of the transistor for the zero-sync method occur in the following order: the active state, the STS, and the ZSS. On the other hand, in the same interval, the conventional method utilizes switching states in the following order: the active state, the first ZSS, the STS, and the second ZSS. Consequently, the conventional method utilizes the additional ZSS depicted by the shaded surfaces in Figure 2b. This additional switching state implies two additional switching transitions of the transistor: the turn-off transition from the active state into the ZSS, and the turn-on transition from the ZSS into the STS. The number of the additional switching transitions increases with the frequency modulation index, which is defined as the ratio between the switching frequency (f_{sw}) and the fundamental frequency of the reference voltages (f). The described additional transitions also occur in the lower transistor pulse (S_{A-}) during the interval when the instantaneous value of v_{refA} is lower than the values of v_{refB} and v_{refC}. Finally, compared to the conventional method, in the zero-sync method, each transistor in the inverter bridge utilizes two switchings less per switching period during one third ($2\pi/3$) of the fundamental period of the reference signal. Consequently, the total number of switchings in the inverter bridge during each fundamental period ($1/f$) is reduced by

$$N_{red} \approx 6\frac{2}{3}\frac{f_{sw}}{f} = 4M_f \tag{4}$$

It is determined that N_{red} calculated according to (4) corresponds to the actual number of reduced switchings when the amplitude modulation index M_a is equal to or greater than 1 or M_f is the integer multiple of 3. Otherwise, N_{red} calculated by (4) is slightly lower (i.e., by up to five) than the actual number of reduced switchings. However, this is a negligible error given that M_f in common applications varies from 50 to 500 [29].

As a result of the reduced switching, the switching losses are lower in the case of the zero-sync method, whereas the conduction losses remain the same since the total duration of the ZSS within each T_{sw} is the same for both the considered methods.

An increase of the D_0 value, with the applied constant M_a, would lead to a shorter duration of the additional ZSS. Therefore, the question arises whether the additional ZSS would disappear if D_0 would reach $D_{0,max}$. The answer to this is provided in Figure 3, where the same waveforms as in Figure 2 are shown for the case $D_0 = D_{0,max}$. Figure 3 proves that the additional ZSS still exists even in this case, although its duration is very short. Finally, it may be concluded that the difference in the switching states distribution between the zero-sync method and the conventional method always exists, regardless of the D_0 value.

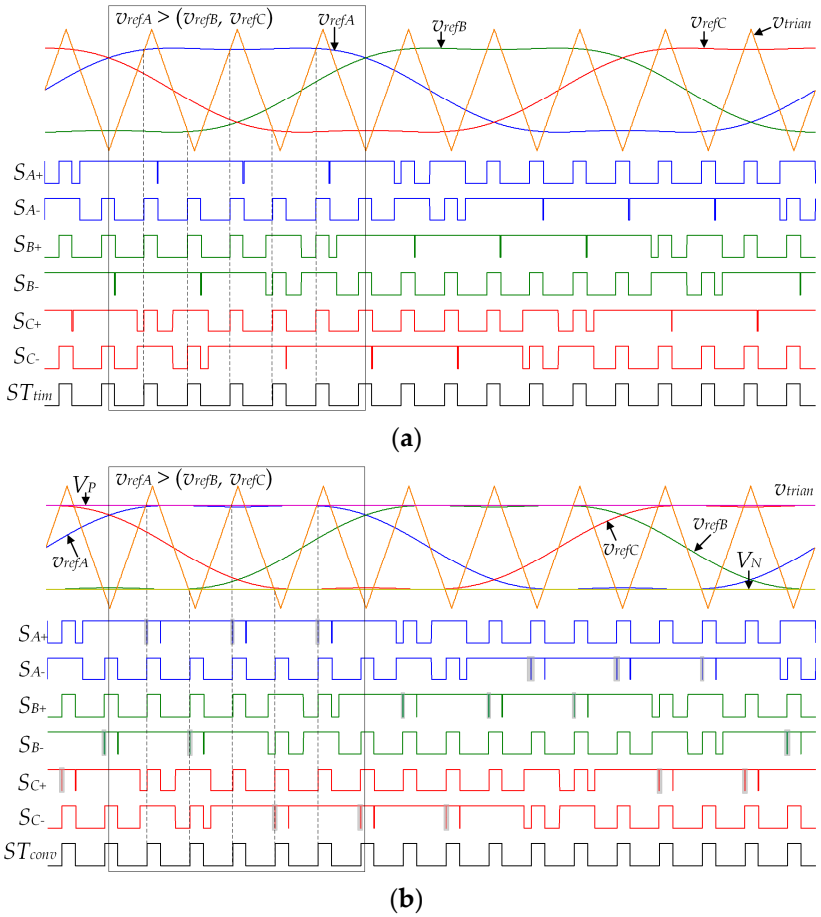


Figure 3. Waveforms of the zero-sync STS injection method (**a**) and the conventional STS injection method (**b**), with $D_0 = D_{0,max}$.

4. Hardware Implementation

The logic diagram of the PWM pulses generation with the STS injection for both the zero-sync and conventional methods is shown in Figure 4. The SPWM pulses are generated by means of the MicroLabBox (dSpace) microcontroller, whereas the corresponding control algorithm was built in the Matlab-Simulink. As for the zero-sync method, the ZSSs are detected by considering all the SPWM pulses. The logic signal (ZS) shown in Figure 4 equals 1 during the zero SPWM state, otherwise it equals 0. The SPWM pulses for the upper transistors (S_{A+}, S_{B+}, S_{C+}) and those for the lower transistors (S_{A-}, S_{B-}, S_{C-}) are fed into the respective OR gates. The output signals of the two OR gates are fed into the NAND gate, which, in turn, generates the ZS signal at its output. The ZS value for all the possible combination of the SPWM pulses is given in Table 1. It is notable that the ZS signal may be correctly obtained by utilizing a single logic XNOR gate for the upper transistor signals (S_{A+}, S_{B+}, S_{C+}) or the lower transistors signals (S_{A-}, S_{B-}, S_{C-}). However, this method was not utilized due to the later introduction of the dead-time, as described in Section 6. The rising pulse of ZS (i.e., from 0 to 1) initiates the timer: the logic STS signal (ST_{tim}) is set to value 1, which marks the start of the STS. The duration of the STS is equal to half of the STS period ($T_0/2$). At the end of the STS, defined by the timer operation, ST_{tim} becomes 0 and retains that value until the next STS. As for the conventional method, the corresponding logic STS signal (ST_{conv}) is the result of the logic OR operation of the signals S_P and S_N, which are obtained as the result of comparison of the reference voltages V_P and V_N with v_{trian}. The STS signal (ST_s), which is in the end injected into the six SPWM pulses by means of the respective logic OR gates, is the result of the logic OR operation of the signals ST_{tim} and ST_{conv}. However, it is important to note that when the zero-sync method is implemented, ST_{conv} is permanently set to zero. Likewise, when the conventional

method is implemented, ST_{tim} is permanently set to zero. The output PWM pulses (S^*_{A+}, S^*_{A-}, S^*_{B+}, S^*_{B-}, S^*_{C+}, S^*_{C-}) are, in fact, the SPWM pulses with the injected STSs.

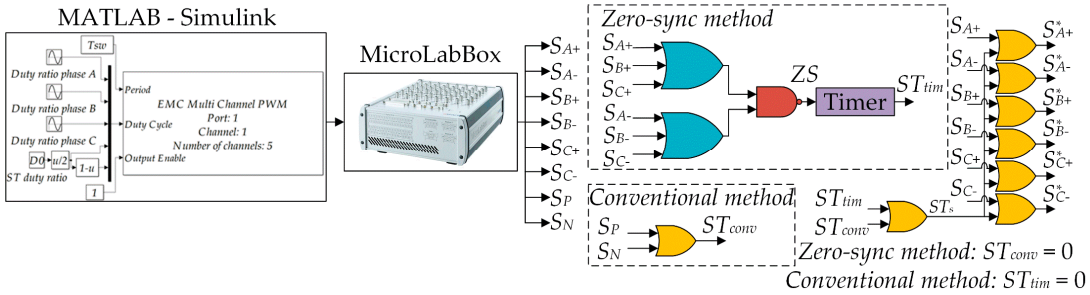


Figure 4. Logic diagram of the PWM pulses generation with the STSs injection by means of both the zero-sync and conventional methods.

Table 1. The available SPWM pulses combinations and the *ZS* signal value.

S_{A+}	S_{B+}	S_{C+}	S_{A-}	S_{B-}	S_{C-}	*ZS*
0	0	0	1	1	1	1
0	0	1	1	1	0	0
0	1	0	1	0	1	0
0	1	1	1	0	0	0
1	0	0	0	1	1	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Figure 5 shows the electrical scheme of the circuitry utilized for the STS injection by means of both the considered methods. The circuitry was built based on the logic diagram, so the colors of the components in Figure 5 correspond to those in Figure 4. The logical 0 in the logic diagram corresponds to 0 V in the electrical circuitry, whereas the logical 1 corresponds to +5 V. The supply voltage of the circuitry (V_{cc}) was set to +5 V. The *ZS* signal required for the implementation of the zero-sync method is generated by the means of the logic OR gates SN74AC32N (Texas Instruments) along with the logic AND gate 74HC08AP (Texas Instruments) and the logic inverter. The latter is realized by utilizing the NPN bipolar junction transistor (BJT1) 2N3904 (Texas Instruments). The resistors R_{b1} = 10 kΩ and R_{c1} = 1 kΩ shown in Figure 5 are utilized in the base and collector circuit of the BJT1, respectively, to ensure adequate BJT1 currents.

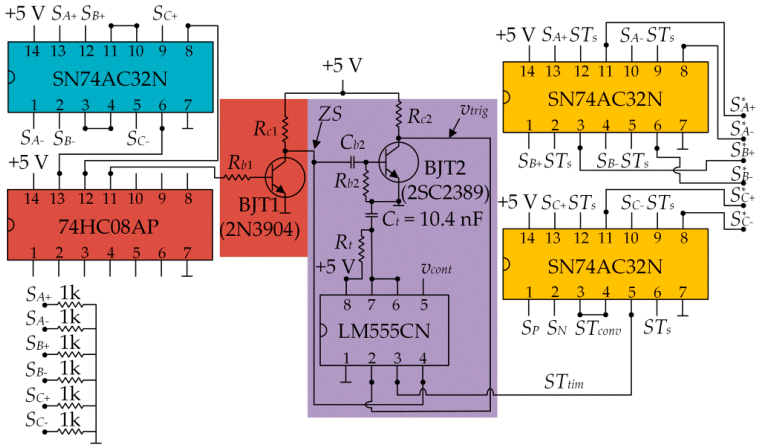


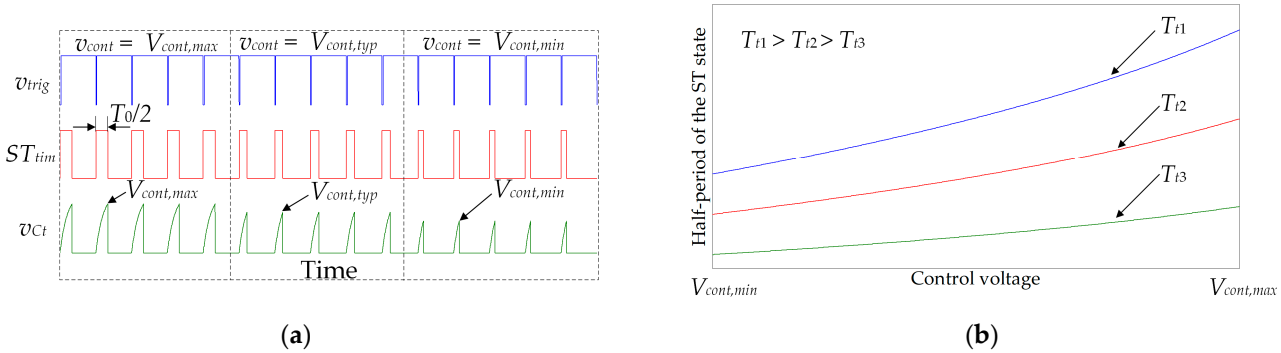
Figure 5. Electrical diagram of the PWM pulses generation with the STSs injection by means of both the zero-sync and conventional methods.

A monostable operation mode of the timer LM555CN (Texas Instruments) is implemented in order to ensure desired half STS period ($T_0/2$) in the zero-sync method. In this operation mode, the timer output (pin 3), which is utilized as the signal ST_{tim}, is set to +5 V in the case when the voltage value of 0 V is applied to the trigger input (pin 2). The trigger input signal (v_{trig}) is generated by utilizing the NPN BJT2 2SC2389 (Rohm). At the beginning of the ZSS, the BJT1 turns off which causes the ZS value to become +5 V. The current instantaneously starts to flow from the supply terminal (+5 V) through R_{c1} and C_{b2} = 100 pF into the base of the BJT2. That initiates the start of C_{b2} charging and the BJT2 turns on (note that R_{c2} = 5.6 kΩ ensures adequate BJT2 collector current), which results in v_{trig} = 0 V. This triggers the timer and the ST_{tim} value changes to +5 V, which represents the start of the STS. As a result, the timer pins 6 and 7 internally disconnect from the pin 1, which is connected to the ground. Therefore, the capacitor C_t, connected between the timer pins 6 and 7 and the ground, begins to charge through the resistor R_t, connected between the timer pins 8 (supply +5 V) and 6 and 7. During the STS, the v_{trig} value remains 0 V as long as the base current is high enough to maintain the BJT2 turned on, practically until C_{b2} is fully charged. Once C_{b2} is fully charged, the BJT2 turns off and the v_{trig} value becomes +5 V. In the considered circuitry, the v_{trig} value remains 0 V for approximately 1.5 µs within each ZSS, which is determined by the time constant $R_{c1}C_{b2}$ and BJT2 parameters such as the base-collector voltage and the current transfer ratio of the base current. The value of the timer output (ST_{tim}) remains +5 V until the voltage across C_t (v_{Ct}) reaches the value of the signal applied to the timer pin 5 (v_{cont}). At that point, the ST_{tim} value becomes 0 V (STS ends) and retains that value until the next STS. As the ST_{tim} value changes to 0 V, the timer pins 6 and 7 internally connect to the pin 1 (ground) and thus enable C_t discharge. Note that for the proper operation of the timer, the v_{trig} value has to be +5 V at the moment when v_{Ct} reaches v_{cont}. Therefore, each STS generated by the timer in considered circuitry has to last longer than 1.5 µs. Finally, at the end of the ZSS, the BJT1 turns on, the ZS value changes to 0 V, and C_{b2} discharges through R_{b2} = 10 kΩ and BJT1. In this way, the multiple trigger occurrences within a single ZSS are prevented. The implemented circuitry allows the STS to last equal or lower than the ZSS. This is achieved by utilizing the ZS signal to control the reset of the timer (pin 4). If the reset is set to 0 V, the timer output is disabled (pin 3 is permanently set to 0), whereas if the reset is set to +5 V, the timer operates regularly.

The STS signal (ST_s) shown in Figure 5 is injected into the SPWM signals by means of the logic OR gates SN74AC32N. ST_s is the result of the logic OR operation of ST_{tim} and ST_{conv}. ST_{conv} is generated as the result of logic OR operation of S_P and S_N, also by utilizing the logic OR gates SN74AC32N. Note that when the zero-sync method is implemented, the values of S_P and S_N are permanently set to 0 V, whereas when the conventional method is implemented, the v_{cont} value is permanently set to 0 V. Finally, it is important to emphasize that the rise times of the logic gates and the timer of approximately 10 ns and 100 ns, respectively, do not affect the proper operation of the circuitry.

Figure 6a shows the waveforms of v_{trig}, ST_{tim}, and v_{Ct} in the case when the maximum ($V_{cont,max}$), minimum ($V_{cont,min}$), and typical ($V_{cont,typ}$) values of v_{cont} are applied, with constant values of R_t and C_t. These three values of v_{cont}, selected to point out the effect of v_{cont} variation, are defined based on the recommendations given in the datasheet of the timer manufacturer. However, v_{cont} may be varied continuously, with the precision depending on the resolution of the MicroLabBox analog output. The value of v_{Ct} may be calculated based on the supply voltage and the time constant $T_t = R_tC_t$, as follows:

$$v_{Ct} = V_{cc}\left(1 - e^{-\frac{T_0/2}{T_t}}\right) \tag{5}$$



(**a**) (**b**)

Figure 6. Waveforms of the trigger voltage, STS signal generated by the timer, and voltage of C_t (**a**), Half-period of the STS as a function of the control voltage (**b**).

In the considered monostable mode, the ST_{tim} value instantly changes from 1 to 0 when v_{Ct} reaches v_{cont}. Hence, the value of $T_0/2$ may be calculated based on (5), with applied $v_{Ct} = v_{cont}$, as follows:

$$T_0/2 = -T_t \ln\left(1 - \frac{v_{cont}}{V_{cc}}\right) \tag{6}$$

In this study, the value of V_{cc} is set to 5 V which results with $V_{cont,max}$ = 4 V and $V_{cont,min}$ = 2.6 V according to the recommendations given in the datasheet of the timer manufacturer. By considering the values of $V_{cont,min}$ and $V_{cont,max}$, the maximum ($T_{0,M-tim}/2$) and minimum ($T_{0,m-tim}/2$) values of $T_0/2$ may be defined as follows:

$$\begin{aligned} T_{0,M-tim}/2 &= -T_t \ln\left(1 - \tfrac{4}{5}\right) = 1.61T_t \\ T_{0,m-tim}/2 &= -T_t \ln\left(1 - \tfrac{2.6}{5}\right) = 0.73T_t \end{aligned} \tag{7}$$

The scope of $T_0/2$ variation depends on the value of the time constant (T_t), wherein the $T_{0,m-tim}/2$ value has to be higher than 1.5 µs, as explained before. Figure 6b shows $T_0/2$ as a function of v_{cont} for different values of T_t. The minimum and maximum values of $T_0/2$, which may be achieved by the timer, define the scope of the STS duty ratio variations. The minimum ($D_{0,m-tim}$) and maximum ($D_{0,m-tim}$) duty ratios are defined as follows:

$$\begin{aligned} D_{0,M-tim} &= \frac{2T_{0,M-tim}/2}{T_{sw}} = 3.22\frac{T_t}{T_{sw}} \\ D_{0,m-tim} &= \frac{2T_{0,m-tim}/2}{T_{sw}} = 1.46\frac{T_t}{T_{sw}} \end{aligned} \tag{8}$$

Hence, due to fact that the range of D_0 variation is limited according to (8), all D_0 values in the range of 0 to $D_{0,max}$ may not be achieved by utilizing the timer. This is not a huge disadvantage since in most applications such a broad scope of D_0 is not required [13–17]. In order to achieve the desired scope of D_0 variation for the certain value of T_{sw}, the value of T_t has to be determined from (8).

Note also that the described electrical circuitry allows the implementation of the SPWM with omitted STSs. To achieve that, the values v_{cont}, S_P, and S_N have to be permanently set to 0 V. In this way, the considered electrical circuitry does not generate the STSs. The described electrical circuitry also allows the implementation of the simple-boost SVPWM method, proposed in [7].

Figure 7 shows the photo of the electrical circuitry whose electrical diagram is shown in Figure 5. The input SPWM pulses along with the signals S_P and S_N are connected to the digital output ports of the MicroLabBox, whereas the output PWM pulses are connected to the gate drivers of the transistors. The control voltage (v_{cont}) is connected to the board from the analog output of the MicroLabBox by means of a coaxial cable. Note that C_t is fixed to the board, whereas R_t may easily be removed and replaced by the resistor

of another resistance value. Thus, the desired value of T_t, which ensures the desired scope of D_0 variation, is achieved by applying R_t with the required resistance value to the board. In order to prevent problems with the dirty ground, the ground pins of all the logic gates are connected to the copper plate placed underneath the main board. Moreover, the electromagnetic interference (EMI) was suppressed by accommodation of the board into the housing BIM2001/11-EMI/RFI (Camdenboss).

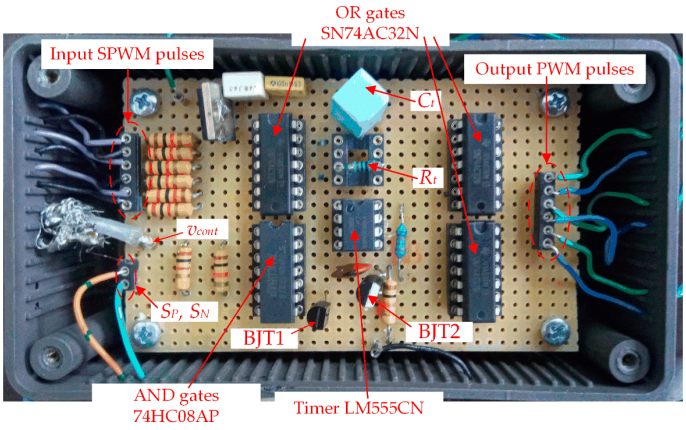


Figure 7. Photo of the electrical circuitry utilized for the STSs injection.

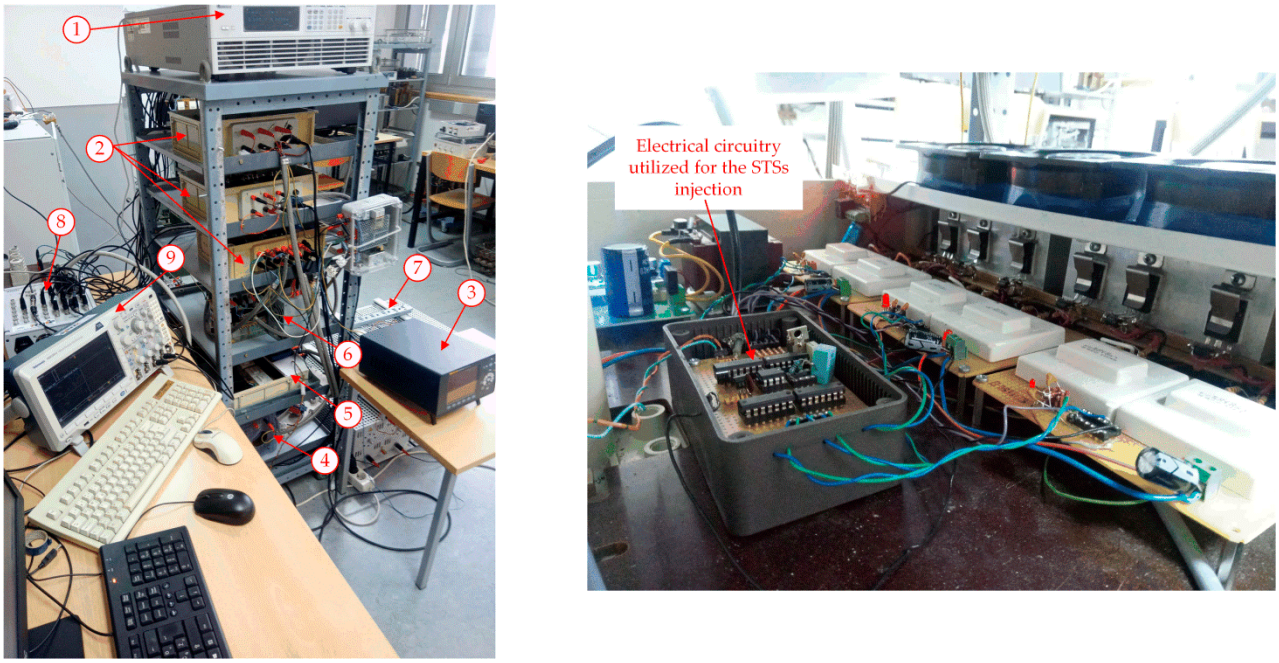
5. Experimental Evaluation of the Zero-Sync Method

Figure 8a shows the laboratory setup of the system used for the experimental evaluation of the zero-sync method. The main components are denoted as follows:

1. DC power supply Chroma 62050H 600S, voltages up to 600 V, currents up to 8.2 A.
2. Hall-effect transducers LA 50-P/S55 (for the qZSI input current and the output phase current), DVL 500 (for the qZSI voltages), and CV 3–500 (for the ac load voltage) (LEM).
3. Power analyzer Norma 4000 (Fluke), used for the measurement of the output load power.
4. qZSI impedance network built of inductors with powder cores T520-26 (Micrometals) ($L_1 = L_2 = 20.2$ mH (unsaturated), $R_L = 0.5\ \Omega$ (at 25 °C)), polypropylene capacitors MKSPI35-50U/1000 (Miflex) ($C_1 = C_2 = 50$ µF, ESR = 7.8 mΩ), and the diode which was built as a serial compound of three diode sets, where each set was built as a parallel compound of three FWDs of the IGBT-FWD pair IRG8P25N120KD (International Rectifier).
5. qZSI three-phase inverter bridge (IXBX75N170 IGBTs (IXYS) and SKHI 22B(R) drivers (Semikron)) shown in Figure 8b.
6. LCL filter at the qZSI output stage ($L_{f1} = 8.64$ mH, $L_{f2} = 4.32$ mH, $C_f = 4$ µF, $R_d = 10\ \Omega$).
7. Variable resistors utilized as a symmetric three-phase load.
8. MicroLabBox controller board (dSpace) for the qZSI control.
9. Oscilloscope MDO 3014 (Tektronix).

The considered laboratory setup was built to operate in the stand-alone configuration with the switching frequencies in the range 5–10 kHz. The selected IGBTs, shown in Figure 8b, have a sufficiently high collector-emitter break down voltage and nominal collector current to ensure proper operation of the qZSI. They were utilized instead of metal oxide semiconductor field effect transistors (MOSFETs) due to the lower level of electromagnetic interference [30]. On the other hand, IGBTs have somewhat higher switching losses compared to MOSFETs. The impedance network diode was built as the above-described series-parallel combination of six FWDs of the IGBT-FWD pair IRG8P25N120KD (International Rectifier), thus reducing both the current and voltage stress of the FWDs. The values of the inductors and capacitors in the symmetric impedance network have been chosen to ensure acceptable inductor current ripple in the considered switching frequency range. As for the output LCL filter, the value of the capacitors has been chosen in order to keep the reactive power under 5% of the nominal inverter power of 4 kW. The values of

the damping resistances (R_d), required to avoid the resonance, have been chosen according to the recommendations in [31]. The value of the LCL filter inductors has been chosen in order to ensure acceptable THD of the inverter output current.



(**a**) (**b**)

Figure 8. Laboratory setup of the qZSI in the stand-alone configuration (**a**), the qZSI three-phase inverter bridge (**b**).

The control algorithm of the qZSI was executed with the sampling frequency of 10 kHz. The qZSI was operated in the open-loop mode, meaning that the RMS value of the fundamental load phase voltage was not controlled, whereas its frequency was set to 50 Hz by means of the SPWM. All the experiments were carried out with the three-phase resistive load connected to the inverter output.

The values of $D_{0,max}$ and M_a utilized during the measurements were determined according to the MCBC method and the maximum allowed value of V_{pn}. The maximum V_{pn} value of 1200 V was selected in order to avoid high levels of the electromagnetic interference, disrupting the normal operation of the gate drivers. The maximum applied qZSI input voltage amounted to 500 V, which along with V_{pn} = 1200 V defines $D_{0,max}$ = 0.29 according to (2). Finally, the M_a value of 0.819 is obtained according to (3). For the M_a value higher than 0.819, the V_{pn} value would surpass 1200 V for the corresponding $D_{0,max}$ value, whereas for the M_a value lower than 0.819, the V_{pn} value would stay below 1200 V for D_0 in the range $0 < D_0 < D_{0,max}$.

The switching frequencies in the range 5–10 kHz were considered during the measurements. R_t values of 1 kΩ and 2 kΩ were utilized with C_t fixed to 10.4 nF in order to ensure the desired values of $T_0/2$ for all the considered switching frequencies. Figure 9 shows $T_0/2$ as a function of the control voltage (v_{cont}) for the two utilized values of R_t. It is notable that the experimentally measured values of $T_0/2$ almost perfectly match those obtained by (6) for both the considered resistance values. Table 2 shows the available range of variation of the duty ratio value, as per (8), for all the considered switching frequencies and for the two applied R_t values.

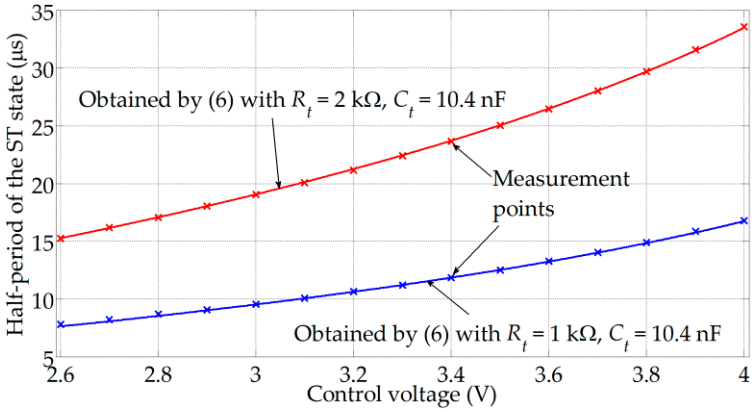


Figure 9. Half-period of the STS as a function of the control voltage obtained for the considered experimental setup.

Table 2. The available range of variation of the duty ratio value obtained for the two utilized values of R_t resistance.

Switching Frequency	R_t = 1 kΩ		R_t = 2 kΩ	
	$D_{0,m\text{-}tim}$	$D_{0,M\text{-}tim}$	$D_{0,m\text{-}tim}$	$D_{0,M\text{-}tim}$
5 kHz	0.07	0.17	0.15	0.33
6 kHz	0.09	0.2	0.18	0.4
7 kHz	0.1	0.23	0.21	0.47
8 kHz	0.12	0.27	0.24	>0.5
9 kHz	0.13	0.3	0.27	>0.5
10 kHz	0.15	0.33	0.3	>0.5

The experimental evaluation of the zero-sync method was carried out through the comparison with the conventional method. First, the respective waveforms were compared in order to highlight the differences in the switching states distribution between the two considered methods. Figure 10a,b show the respective experimental waveforms of the collector-emitter voltage of the upper transistor in the phase A ($v_{ce,A+}$), the qZSI input current (i_{L1}), and the reference voltage in the phase A (v_{refA}) for a single fundamental period of v_{refA}. The measurements were carried out with f_{sw} = 5 kHz, D_0 = 0.24, M_a = 0.819, v_{in} = 500 V, and the load power set to 1000 W. The waveforms were recorded by the oscilloscope MDO 3014 (Tektronix). The part of the v_{refA} period with notable differences between the two considered injection methods is additionally magnified (lower part of Figure 10a,b). The transistor switching state may be detected based on the value of $v_{ce,A+}$: when $v_{ce,A+}$ value is approximately 0, the transistor is turned on, whereas it is turned off otherwise. On the other hand, the i_{L1} waveform was utilized for the detection of the STSs: during the STS, i_{L1} increases, whereas it decreases otherwise. The inductor current ripple for both the considered methods is practically the same and amounts to approximately 46% of the mean value. The calculated value of the current ripple obtained as $V_{C1}T_0/2L$—the equation given in [15]—amounts to 37% of the mean value. The V_{C1} value of approximately 770 V was determined according to the corresponding waveforms shown in Figure 11, whereas the inductance value was determined according to the equation given in [32], which is based on the mean value of the inductor current (I_{L1}).

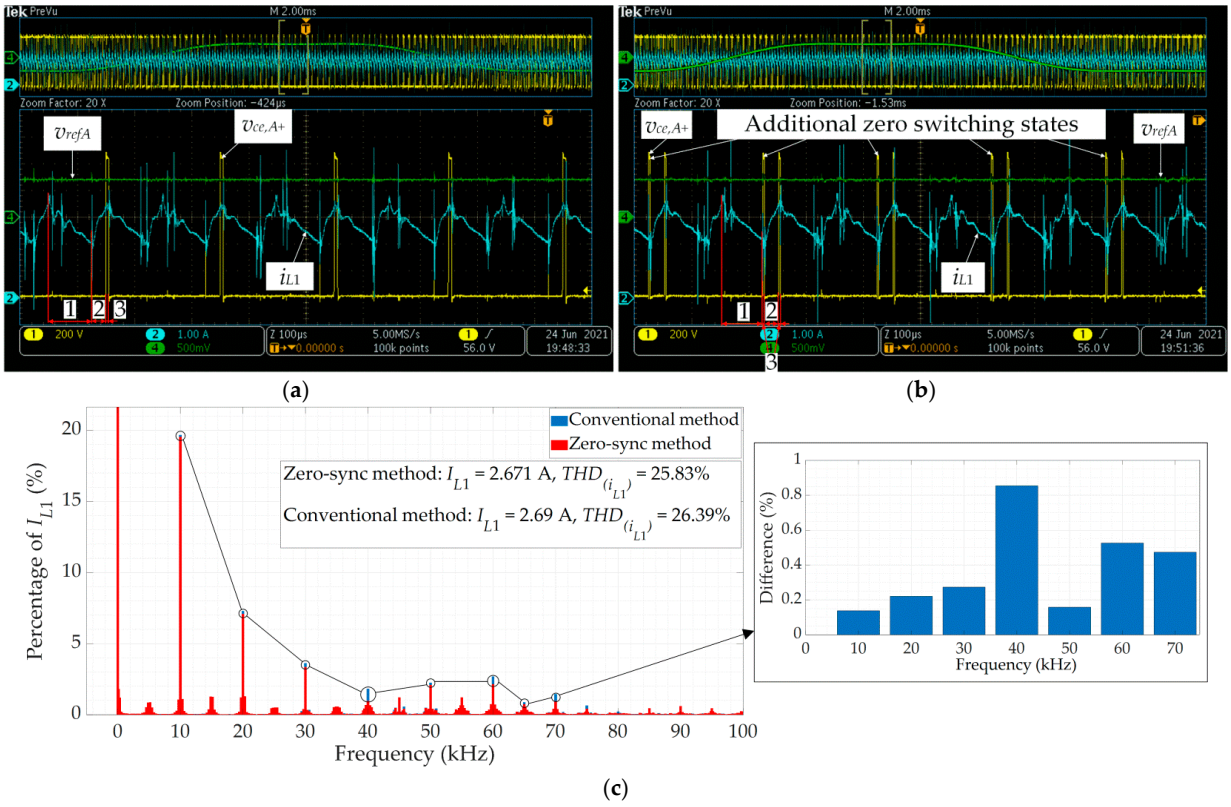


Figure 10. Waveforms of the reference voltage of phase A, collector-emitter voltage of the upper transistor in the phase A, and qZSI input current in case of implementing the zero-sync method (**a**) and the conventional method (**b**), the harmonic spectrum of the qZSI input current waveform (**c**).

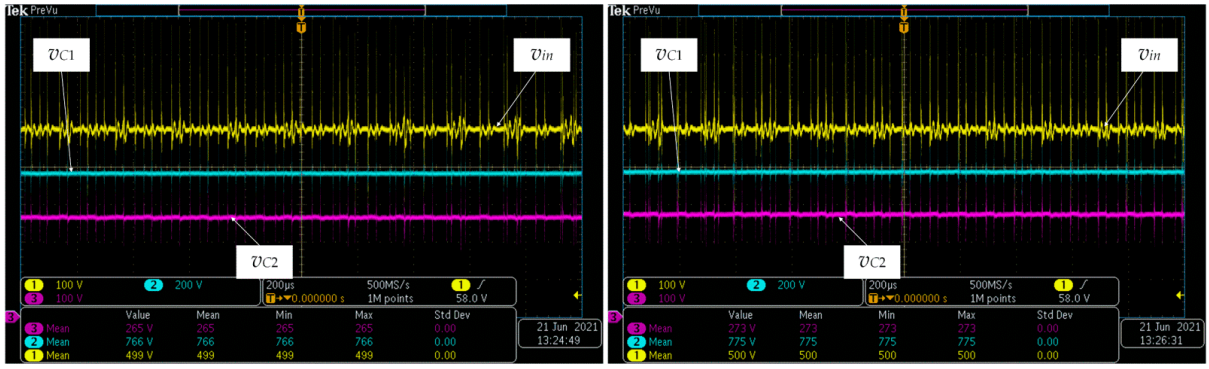


Figure 11. Waveforms of the input voltage, voltage across the capacitor C_1, and voltage across the capacitor C_2: the zero-sync method (**a**) and the conventional method (**b**).

The switching states of the zero-sync method are shown in Figure 10a and occur in the following order: the active state (interval 1), the STS (interval 2), the ZSS (interval 3). As opposed to this, the conventional method, shown in Figure 10b, utilizes an additional ZSS ($v_{ce,A+} \approx 800$ V) in between the active state and the STS. This proves the fact mentioned in Section 3 that the conventional method utilizes the additional ZSS for the transistor A+ (two additional switching transitions) in the interval where $v_{refA} > (v_{refB}, v_{refC})$ applies (similar applies for all the other transistors as well).

Figure 10c shows the harmonic spectrum of the qZSI input current waveform for both the considered methods, where harmonic components are shown as the percentage of the input current dc component. The harmonic components that are integer multiples

of $2f_{sw}$ = 10 kHz are notable since the fundamental frequency of the ac component of the qZSI input current amounts to $2f_{sw}$ (i.e., there are two STSs per switching period). The share of high-order harmonics and the THD are lower in the case of the zero-sync method compared to the conventional method.

The waveforms of the qZSI input voltage and the voltages across the capacitors C_1 and C_2 for both the considered methods are shown in Figure 11. The measurements were carried out with the same input parameters as the measurements shown in Figure 10. The waveforms of all the considered voltages are similar for both the considered methods. However, note that the mean values of the voltages v_{C1} and v_{C2} (V_{C1} = 766 V, V_{C2} = 265 V for the zero-sync method and V_{C1} = 775 V, V_{C2} = 273 V for the conventional method) are higher than the values obtained from (2) based on v_{in} and D_0 (V_{C1} = 731 V, V_{C2} = 231 V). This is the consequence of the unintended additional boost. This, in turn, occurs due to the unintended short circuiting across the inverter legs (i.e., unintended STSs) caused by the non-ideal switching of the involved transistors, as discussed later. Likewise, the mean values of v_{C1} and v_{C2} are higher for approximately 10 V in the case of the conventional method compared to the zero-sync method due to the higher overall number of switchings and, consequently, higher number of unintended STSs. This unintended additional boost was eliminated by introducing the dead-time, which is shown in the next section.

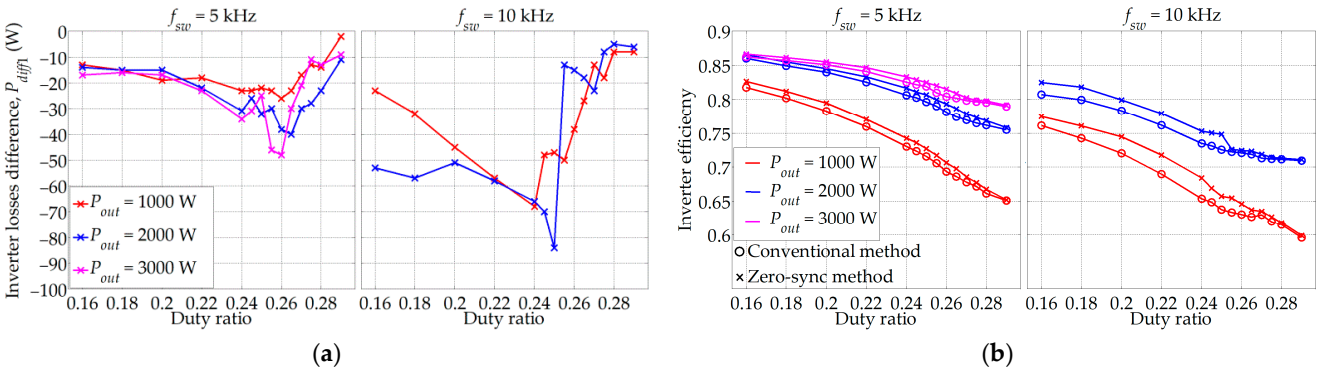
Based on the waveforms shown in Figures 10 and 11, it may be concluded that there are no notable differences in terms of the EMI noises between the two considered methods. In order to achieve a satisfying trade-off between the EMI noises and the switching losses of the IGBTs, the gate turn-on and turn-off resistances were both set to 15 Ω. Detailed analysis of the EMI noises exceeds the scope of this study, but it may be assumed that the EMI noises are somewhat lower in the case of the proposed zero-sync method due to the lower overall number of switchings compared to the conventional method.

The difference in the switching states distribution between the two considered STS injection methods results in the inverter losses difference and, thus, the efficiency difference. For the purpose of inverter losses and efficiency measurement, the inverter input power was measured by Chroma, whereas the output load power was measured by the high-precision power analyzer Norma 4000 (Fluke). The inverter losses ($P_{l-zsm/conv}$) for the zero-sync method (subscript "*zsm*") and the conventional method (subscript "*cm*") were obtained as

$$P_{l-zsm/cm} = P_{in-zsm/cm} - P_{out-zsm/cm} \tag{9}$$

where $P_{in-zsm/cm}$ is the inverter input power and $P_{out-zsm/cm}$ is the load power.

Figure 12 shows the inverter losses difference and the efficiency as a function of the duty ratio for different values of the load power and for the switching frequencies of 5 kHz and 10 kHz, with M_a = 0.819 and V_{in} = 500 V. The inverter losses difference (P_{diff1}) shown in Figure 12a, obtained as P_{l-zsm}–P_{l-cm}, is negative for all the considered values of D_0, meaning that the inverter losses are lower in the case of the zero-sync method.



(**a**) (**b**)

Figure 12. Inverter losses difference (P_{diff1}) (**a**) and inverter efficiency (**b**) as a function of the duty ratio for different values of the load power and switching frequency.

It is notable that P_{diff1} varies with respect to the duty ratio. For example, for f_{sw} = 5 kHz, it may be noted that the absolute value of P_{diff1} increases with D_0 in the range from 0.16 to about 0.26, and then it rapidly decreases. The described behavior of the inverter losses difference is related to the additional transistor switching occurring in the conventional STS injection method. The additional switching implies higher switching losses of the transistor. For $D_0 \leq 0.26$, the duration of the additional ZSS is long enough to ensure both the mentioned switching transitions of the transistor to be finished completely. Hence, in this region, the switching losses of the transistors are dominant and increase with D_0 [33] due to the increase of V_{pn} as per (2). However, when the applied D_0 is higher than 0.26, the turn-on transition into the STS occurs before the previous turn-off transition from the active state into the ZSS has completely finished. This leads to a decrease of the corresponding switching losses, and consequently to a decrease of the P_{diff1} absolute value. It is important to note that, in case $D_0 = D_{0,max}$ is applied, P_{diff1} is still negative, which confirms the claims stated in the last paragraph of Section 3.

The similar behavior of P_{diff1} with regard to the variation of D_0 was noted for f_{sw} = 10 kHz (right part of Figure 12a). However, the absolute values of P_{diff1} were in this case somewhat higher due to the increase of the switching transitions with f_{sw} and, hence, the increase of the switching losses. Note that the absolute value of P_{diff1} increases with D_0 until the turning point ($D_0 \approx 0.24$), which is in this case slightly lower compared to the previous example at f_{sw} = 5 kHz. This is related to the fact that the switching transitions occur more often at higher switching frequencies. However, since each transition of the transistor requires a certain amount of time to be executed, depending solely on its current and voltage, the inability of the transistor to completely turn-off from the active state into the ZSS occurs for lower values of D_0 compared to the example at f_{sw} = 5 kHz.

The variation of the load power did not have a clear impact on the inverter losses difference. This may be explained by the fact that the increase of the load power primarily leads to the increase of the transistor conduction losses, whereas the increase of the switching losses remains less pronounced [33]. Note also that the load power of 3000 W was not achieved for f_{sw} = 10 kHz for both the considered methods because this would cause the case temperature of the IGBT-diode pair to surpass the maximum allowed temperature, set to 130 °C. This may ultimately destroy the device.

Figure 12b shows the inverter efficiency for the two considered STS injection methods. As expected, the inverter efficiency is higher in the case of the zero-sync method and it increases with the load power. The highest efficiency difference is noted for D_0 = 0.2 and f_{sw} = 10 kHz and amounts to approximately 4%. In addition, the inverter efficiency for both the considered methods decreases with D_0 increase due to the increase of V_{pn} according to (2), which, in turn, implies higher switching losses. Moreover, lower efficiency is noted for the higher switching frequency, regardless of the applied STS injection method, which is again due to the higher switching losses.

Figure 13 shows the inverter losses difference and the efficiency as a function of the duty ratio for different values of the input voltage and the switching frequencies of 5 kHz and 10 kHz, with M_a = 0.819 and P_{out} = 1000 W. The variation of the inverter losses with respect to D_0 in Figure 13a is practically the same as in Figure 12a. However, the variation of the input voltage (V_{in}) significantly affects the inverter losses difference. Note that by reducing the input voltage by 100 V, the absolute value of P_{diff1} is about two times reduced. This is the consequence of V_{pn} decreasing with V_{in} according to (2), which in turn leads to the decrease of the switching losses. This effect is more pronounced at the higher switching frequency.

Figure 13b shows that the input voltage decrease favorably affects the inverter efficiency, primarily due to the decrease of the switching losses. The negative sign of P_{diff1} for all the considered values of D_0 and V_{in} implies that the zero-sync method ensures higher inverter efficiency compared to the conventional method. The smallest efficiency difference is observed for V_{in} = 300 V and f_{sw} = 5 kHz and amounts to 0.5%, whereas the largest is observed for V_{in} = 500 V and f_{sw} = 10 kHz and amounts to 2.5%.

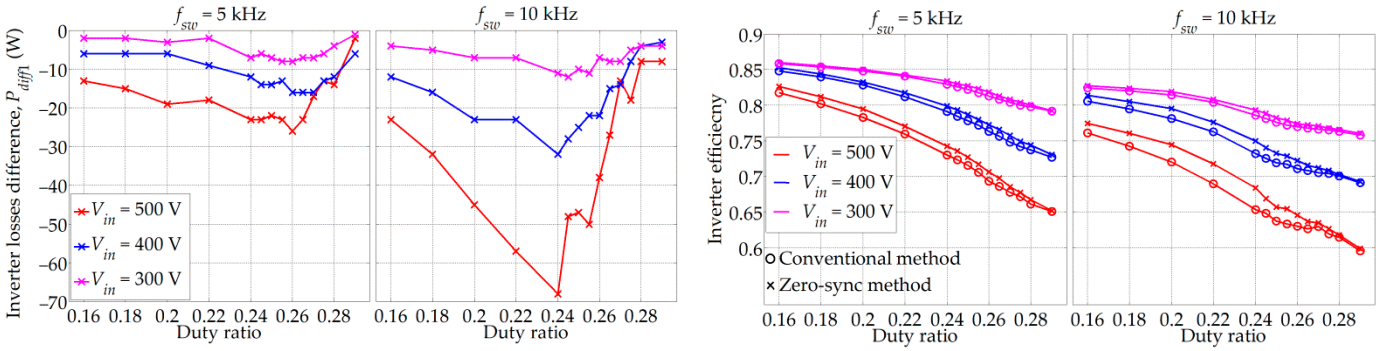


Figure 13. Inverter losses difference (P_{diff1}) (**a**) and inverter efficiency (**b**) as a function of the duty ratio for different values of the inverter input voltage and switching frequency.

Figure 14a shows P_{diff1} as a function of the duty ratio for different values of the switching frequency, with M_a = 0.819, P_{out} = 1000 W, and V_{in} = 500 V. It may be concluded that the absolute value of P_{diff1} increases with the switching frequency, which was expected due to the increased number of switching transitions, and hence the increased switching losses. Note that the turning point of P_{diff1}, after which the absolute value of P_{diff1} starts to decrease with the increase of D_0, occurs for lower D_0 values as f_{sw} increases.

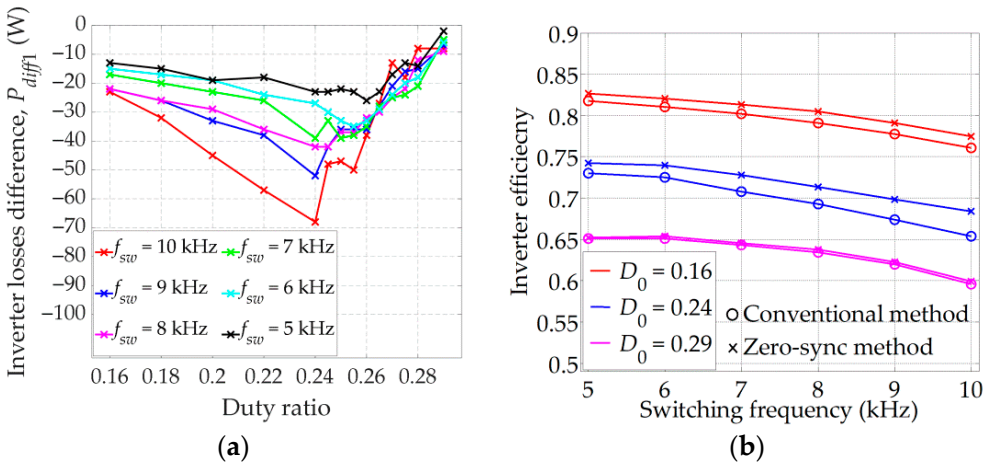


Figure 14. Inverter losses difference (P_{diff1}) as a function of the duty ratio for different switching frequencies (**a**); inverter efficiency as a function of the switching frequency for different duty ratio values (**b**).

The inverter efficiency as function of the switching frequency, for the two considered STS injection methods, is shown in Figure 14b. Three values of D_0 were considered–0.16, 0.24, and 0.29–with M_a = 0.819, P_{out} = 1000 W, and V_{in} = 500 V. The inverter efficiency increases with the decrease of D_0 as well as with the decrease of f_{sw}, both due to the decrease of the switching losses. Note that the zero-sync method results in higher inverter efficiency for all the considered measurement points. The largest difference is noted for D_0 = 0.24 and f_{sw} = 10 kHz and amounts to 4%, whereas the smallest difference is noted for D_0 = 0.29 and f_{sw} = 5 kHz and amounts to 0.4%. This is in accordance with P_{diff1} variation shown in Figure 14a. The absolute value of P_{diff1} for D_0 = 0.24 and f_{sw} = 10 kHz amounts to 70 W, whereas it amounts to only 3 W for D_0 = 0.29 and f_{sw} = 5 kHz.

6. Modified Zero-Sync Shoot-Through Injection Method with the Dead-Time

The experimental comparison of the zero-sync method and the conventional one proved the main advantage of the zero-sync method, which is the inverter efficiency

increase. However, during the experimental investigation, differences were noted between the boost factor achieved through STS injection, defined in (1), and the actual boost determined as follows:

$$B_{act} = \frac{1}{1 - 2D_{0,act}} = \frac{1}{1 - 2\frac{V_{C2}}{V_{in}+2V_{C2}}} \tag{10}$$

where $D_{0,act}$ represent equivalent actual duty ratio calculated according to (2).

In the obtained results, the actual boost factor was always higher than the one achieved through the STS injection and this phenomenon was noted for both the considered STS injection methods. This was the result of unintended short circuiting across the inverter legs (i.e., unintended STSs) due to the non-ideal switching of the involved transistors. The dead-time prevents simultaneous conduction of the transistors in the same inverter leg by introducing the time delay into the PWM signals. So far, the dead-time was not implemented for the qZSI since it is not required due to the existence of the impedance network. However, this does not mean that the transistors in the same leg do not occasionally simultaneously conduct for a short amount of time during the non-STSs. This only means that this sporadic, unintended short circuiting can be tolerated within such a configuration. Hence, although this may not cause the qZSI failure, it results in higher-than-intended and uncontrollable qZSI voltage boost.

Figure 15 shows B_{act} as a function of the introduced dead-time (τ_d) for different applied B values and two switching frequencies, with V_{in} = 500 V, P_{out} = 1000 W, and M_a = 0.819. The actual boost factor rapidly decreases with τ_d increase in the range $0 \leq \tau_d \leq 0.7$ µs for both the considered switching frequencies. This is because the duration of the additional, unintended short circuit occurrences is reduced by introducing the dead-time. Note that the actual boost is significantly higher in the case when the switching frequency is set to 10 kHz as compared to 5 kHz. This is because the higher f_{sw} implies lower T_{sw}, so the time share of the additional short circuits within a single T_{sw} increases. On the other hand, the increase of the actual boost factor with the dead-time is noted for $\tau_d > 0.7$ µs for both the considered switching frequencies. This is related to the blocking of the impedance network diode during the non-STSs, which is caused by the dead-time injection. The increase of τ_d implies the decrease of the output voltage and the load power, which, in turn, results with the decrease of the qZSI input current. Therefore, the non-STSs are bound to last longer than the inductor discharging time, causing D_1 to block the current, thus increasing the boost factor [34,35]. Finally, it was decided to introduce the dead-time into the SPWM of the considered qZSI with the optimal value of τ_d selected to be 0.7 µs. This value is high enough to prevent the occurrence of the additional short circuit occurrences during the SPWM switching transitions, whereas the higher values of τ_d would cause the blocking of D_1 and higher distortion of the inverter output voltage.

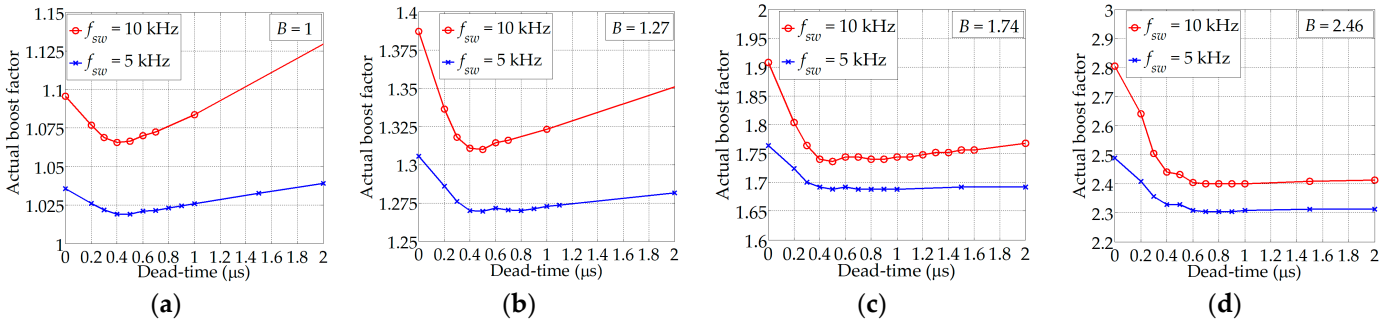
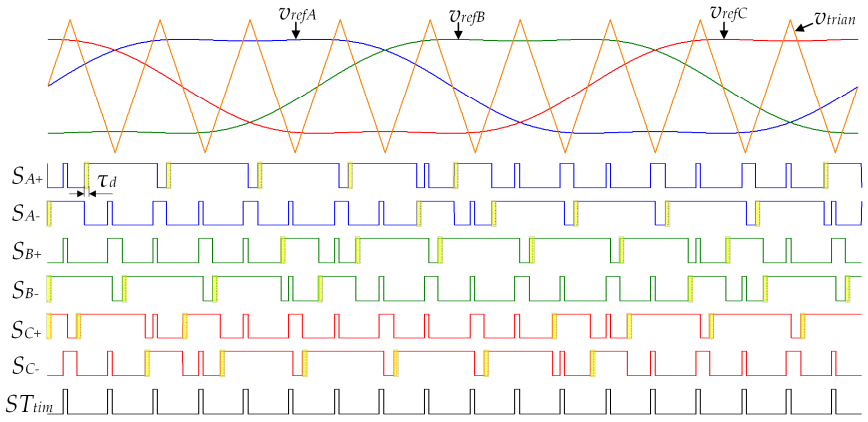


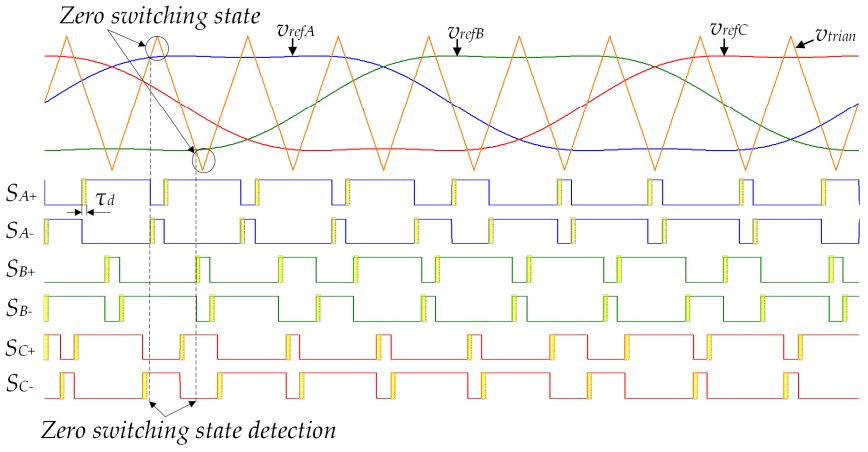
Figure 15. Actual boost factor as a function of the dead-time for applied B = 1 (**a**), B = 1.27 (**b**), B = 1.74 (**c**), and B = 2.46 (**d**).

The modified zero-sync method of STS injection is practically the zero-sync method with the introduced dead-time of optimal duration. Figure 16a shows the characteristic waveforms of the zero-sync method. The dead-time, depicted by the yellow areas in

Figure 16, is injected into the transistor pulses to postpone the turn-on transition into the active SPWM state. This prevents the short circuiting of the corresponding inverter leg during the SPWM switching transitions. However, it may also disrupt the detection of the ZSSs. This can be described by considering the waveforms of the SPWM with introduced dead-time, but with omitted STSs, which are shown in Figure 16b. There are two ZSSs within a single T_{sw}, as is shown in the rectangle in Figure 16b. During the first ZSS, the switching pulses S_{A+}, S_{B+}, and S_{C+} are equal to 0, whereas S_{A-}, S_{B-}, and S_{C-} are equal to 1. However, during the second ZSS, the opposite holds. The first ZSS occurs when the S_{A+} value becomes 0, whereas the second ZSS occurs when the S_{B-} value becomes 0. Thus, the occurrence of the ZSS is in the first case determined by the upper transistor switching pulse and by the lower transistor switching pulse in the second case. The same may be noted within each T_{sw}. That practically means that the first ZSS has to be detected when the switching pulses S_{A+}, S_{B+}, and S_{C+} are equal to 0, whereas the second ZSS has to be detected when the switching pulses S_{A-}, S_{B-}, and S_{C-} are equal to 0. Therefore, the switching pulses of all the transistors needed to be utilized for the detection of the ZSS for the hardware implementation of the modified zero-sync method.



(**a**)



(**b**)

Figure 16. Waveforms of the modified zero-sync method of the STS injection where $0 < D_0 < D_{0,max}$ (**a**), waveforms of the SPWM with the dead-time where the STSs were omitted (**b**).

Figure 17 shows the waveforms of the load phase current in the phase A (i_a) and the qZSI input current (i_{L1}) in the case of implementing the zero-sync method with dead-time. The measurements were carried out with f_{sw} = 5 kHz, D_0 = 0.24, M_a = 0.819, v_{in} = 500 V, and the load power set to 1000 W. The output phase current is practically sinusoidal with the THD of 1.9%. Moreover, by the comparison of the i_{L1} waveforms shown in

Figures 10 and 17, it may be concluded that there is no notable difference in the ripple of the inductor current between all the three methods considered in this paper, namely the zero-sync method with and without dead-time and the conventional method.

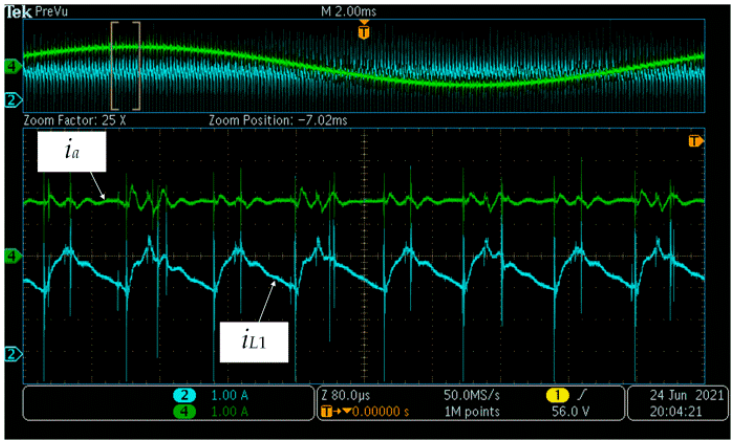


Figure 17. Waveforms of the output load phase current and the qZSI input current in case of implementing the zero-sync method with dead-time.

The evaluation of the zero-sync method with dead-time is provided through the comparison to the zero-sync method without dead-time. The main comparison parameters were the same as those used in Section 5: the power losses difference (P_{diff2}) and the inverter efficiency difference. The inverter losses in the case of the modified zero-sync method (P_{l-mzsm}) were calculated as $P_{in-mzsm} - P_{out-mzsm}$, whereas P_{diff2} was calculated as $P_{l-mzsm} - P_{l-zsm}$.

Figure 18 shows P_{diff2} and the inverter efficiency as a function of the duty ratio for different load power values and the switching frequencies of 5 kHz and 10 kHz, with M_a = 0.819 and V_{in} = 500 V. The inverter losses are significantly reduced by introducing the dead-time, whereas the absolute value of P_{diff2} increases with the load power. The largest absolute value of P_{diff2}, noted for f_{sw} = 10 kHz, D_0 = 0.28, and P_{out} = 2000 W, amounts to 280 W, which results in the inverter efficiency increase of 11%. The lowest absolute value of P_{diff2}, noted for f_{sw} = 5 kHz, D_0 = 0.16, and P_{out} = 2000 W, amounts to 18 W, which results in the inverter efficiency increase less than 1%.

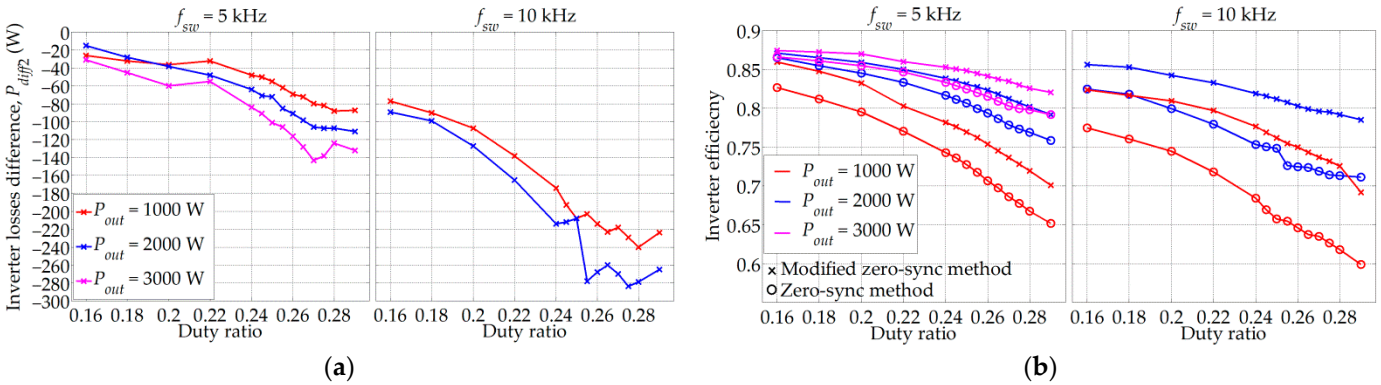


Figure 18. Inverter losses difference (P_{diff2}) (**a**) and inverter efficiency (**b**) as a function of the duty ratio for the different values of the load power and switching frequency.

Figure 19 shows P_{diff2} and the inverter efficiency as a function of the duty ratio for different input voltage values and the switching frequencies of 5 kHz and 10 kHz, with M_a = 0.819 and P_{out} = 1000 W. Note that by reducing the input voltage by 100 V, the absolute value of P_{diff2} is reduced by a factor of two. Likewise, by decreasing the switching

frequency from 10 kHz to 5 kHz, the absolute value of P_{diff2} is again reduced by a factor of two. Therefore, the largest P_{diff2} absolute value of 240 W is noted for f_{sw} = 10 kHz and V_{in} = 500 V (efficiency boost of 10%), whereas the lowest P_{diff2} absolute value of 10 W is noted for f_{sw} = 5 kHz and V_{in} = 300 V (efficiency increase less than 1%).

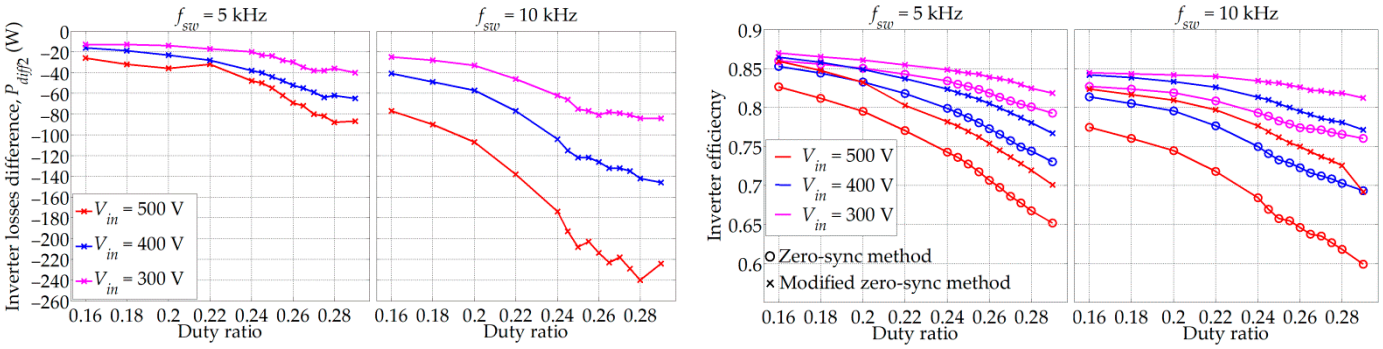


Figure 19. Inverter losses difference (P_{diff2}) (**a**) and inverter efficiency (**b**) as a function of the duty ratio for the different values of the inverter input voltage and switching frequency.

Figure 20a shows P_{diff2} as a function of the duty ratio for different values of the switching frequency, with M_a = 0.819, P_{out} = 1000 W, and V_{in} = 500 V. For the same utilized value of the STS duty ratio, the absolute value of P_{diff2} increases with the switching frequency due to the increase of the switching losses. It is interesting to observe how the mentioned fact affects the inverter efficiency. Figure 20b shows the inverter efficiency as a function of the switching frequency for three values of D_0, namely 0.16, 0.24, and 0.29, with M_a = 0.819, P_{out} = 1000 W, and V_{in} = 500 V. As expected, the inverter efficiency is higher when the dead-time is implemented, with the difference between the two considered methods increasing with D_0. The decrease of the inverter efficiency with the f_{sw} increase noted in the case of the modified zero-sync method is lower compared to the non-modified zero-sync method.

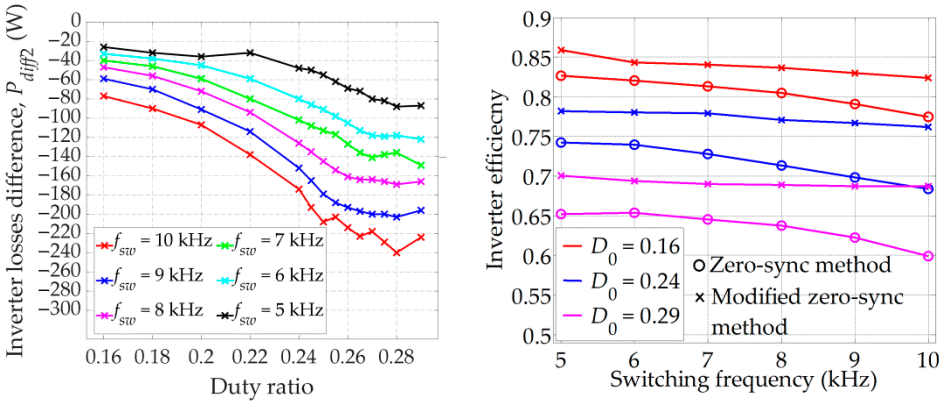


Figure 20. Inverter losses difference (P_{diff2}) as a function of the duty ratio for different switching frequencies (**a**); inverter efficiency as a function of the switching frequency for different duty ratio values (**b**).

The inverter losses differences that occur with regard to different STS injection methods should be reflected in different case temperatures of the utilized IGBT-diode pairs. Therefore, the case temperature of the IGBT-diode pairs was measured in steady state by means of the thermal camera Testo 865 (Testo). Figure 21 shows the case temperature with respect to the duty ratio for all three STS injection methods considered in this study.

Three values of D_0 and three values of the load power were considered for the switching frequencies of 5 kHz and 10 kHz. The highest case temperatures were noted for the conventional method, the zero-sync method resulted with medium temperature values, whereas the implementation of the modified zero-sync method resulted with convincingly the lowest case temperatures. For example, for f_{sw} = 10 kHz, P_{out} = 2000 W, and D_0 = 0.29, the case temperature difference between the modified zero-sync method and the other two methods amounts to approximately 50 °C. Consequently, the implementation of the modified zero-sync method results in an increase of the inverter power rating since the inverter losses and the case temperatures are in this case reduced.

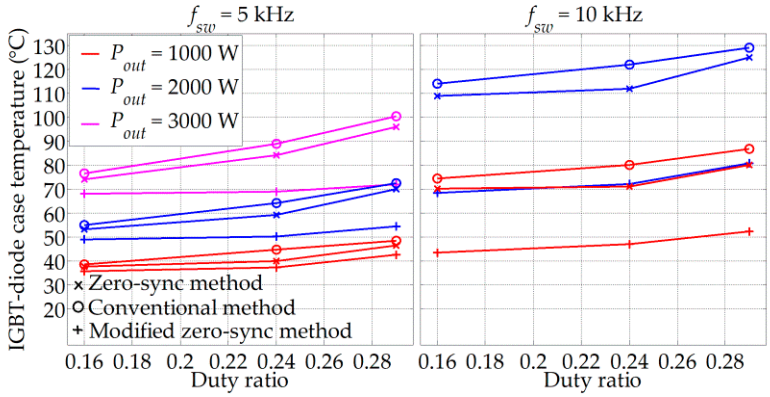


Figure 21. Measured IGBT-diode case temperature as a function of the duty ratio for different load power values.

7. Discussion

The experimental validation of the zero-sync method was caried out through the comparison to the conventional method. The comparison of the corresponding waveforms proved that the total number of switchings in the inverter bridge within a single period of the sinusoidal reference signal is reduced by approximately four times the frequency modulation index (M_f). The comparison of the inverter power losses and efficiency has been carried out for different values of P_{out}, V_{in}, and f_{sw} for D_0 values in a range from 0.16 up to the maximum of 0.29. The inverter power losses have been reduced by 3–85 W in the case of the zero-sync method compared to the conventional method in the tested operating range. Consequently, the inverter efficiency was increased by 0.3–4% in the case of the zero-sync method. The inverter losses difference (P_{diff1}) varies with D_0 variation. The absolute P_{diff1} value increases with D_0 in the range from D_0 = 0.16 to D_0 = 0.24–0.26, where it reaches the maximum value between 8 W and 85 W, and then it rapidly decreases. This behavior is related to the additional transistor switching occurring in the conventional method. For lower values of D_0, the ZSS is long enough to ensure both the mentioned switching transitions of the transistor to finish completely. Since the switching losses of the transistor increase with D_0 due to the increase of V_{pn} as per (2), the absolute inverter power difference increases. However, for higher values of D_0, in the conventional method, the turn-on transition into the STS occurs before the previous turn-off transition from the active into the ZSS has finished. This leads to the decrease of the switching losses in the conventional method and thus to the decrease of the absolute inverter power difference between the two considered methods. The variations in the transistors switching losses have been analyzed with regard to the variation of P_{out}, V_{in}, and f_{sw}. P_{out} has been varied in a relatively narrow range from 1000 W up to 3000 W, leading to low variation of the inverter output current, and thus low variation of the transistors switching losses. On the other hand, the variation of f_{sw} in the range from 5 kHz up to 10 kHz and the variation of v_{in} in the range from 300 V up to 500 V has caused significant variation of the transistors switching losses and thus significant variation of the power losses difference between the two considered methods.

During the experimental investigation, it has been noted that the actual inverter boost factor is always higher than the expected boost factor considering the injected STSs. This was the result of unintended short circuiting across the inverter legs due to the non-ideal switching of the involved transistors. The experimentally determined optimal dead-time of 0.7 μs has been introduced into the SPWM pulses of the zero-sync method to prevent this unintended short circuiting across the inverter legs. As a result, the inverter power losses have been decreased by 15–281 W, resulting in the efficiency increase of 1.5–11%. This has been shown through comparison of the results obtained with the zero-sync method with and without the dead-time. In addition, the case temperatures of the IGBT-diode pairs in the inverter bridge were measured by means of the thermal camera. It turned out that the highest case temperature was noted for the conventional method 129 °C with P_{out} = 2000 W and f_{sw} = 10 kHz, whereas the lowest case temperature was noted for the zero-sync method with implemented dead-time 35 °C with P_{out} = 1000 W and f_{sw} = 5 kHz. These results are in accordance with the previously acquired results obtained by considering the electrical quantities. Finally, the introduction of the dead-time did not affect the inductor current ripple, whereas the output load phase current remained practically sinusoidal with the THD of 1.9%.

8. Conclusions

This paper presents a novel method of STS injection into the three-phase SPWM pulses. The proposed method was successfully applied for the qZSI in the stand-alone operation mode. However, its application is not restricted to this ZSI topology or to stand-alone mode. The developed method was evaluated through the comparison with the conventional method of the STS injection. It turned out that, by implementing the proposed zero-sync method instead of the conventional method, the inverter power losses were decreased, which resulted in the inverter efficiency increase. The maximum noted losses decrease amounted to 85 W, whereas the maximum noted increase of the inverter efficiency amounted to 4%. The additional modification of the zero-sync method was performed by introducing the dead-time of optimal duration. As a result, the qZSI efficiency was increased by up to 11% in the considered operating range. The inverter power losses were reduced in this case by 281 W, whereas the IGBT-diode pair case temperature was reduced by about 50 °C, resulting in a higher achieved power rating of the inverter. The additional benefit of the dead-time introduction is the observed decrease of the inverter electromagnetic interference, but this effect was not quantified in this study.

The drawback of the timer-based implementation of the zero-sync method is the imposed minimum STS duration (1.5 μs in this paper). However, by proper selection of the corresponding hardware components, the minimum imposed STS duration can be adjusted with regard to the minimum required STS duration. In addition, the value of the time constant affecting the STS duration may be varied online by utilizing a digital potentiometer board or a voltage-controlled resistor instead of a constant-value resistor utilized in this study. In the future, it is planned to implement the proposed zero-sync method with dead-time to the qZSI in photovoltaic and wind energy applications with energy storage, for both the stand-alone and grid-tied operation.

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Photovoltaic System with a Battery-Assisted Quasi-Z-Source Inverter: Improved Control System Design Based on a Novel Small-Signal Model

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Abstract: This paper deals with a photovoltaic (PV) system containing a quasi-Z-source inverter (qZSI) and batteries connected in parallel with the qZSI's lower-voltage capacitor. The control system design is based on knowledge of three transfer functions which are obtained from the novel small-signal model of the considered system. The transfer function from the *d*-axis grid current to the battery current has been identified for the first time in this study for the considered system configuration and has been utilized for the design of the battery current control loop for the grid-tied operation. The transfer function from the duty cycle to the PV source voltage has been utilized for the design of the PV source voltage control loop. The PV source voltage is controlled so as to ensure the desired power production of the PV source. For the maximum power point tracking, a perturb-and-observe algorithm is utilized that does not require the measurement of the PV source current, but it instead utilizes the battery current during the stand-alone operation and the *d*-axis reference current during the grid-tied operation. The corresponding tracking period was determined by using the transfer function from the duty cycle to the battery current and in accordance with the longest settling time noted in the corresponding step response. The proposed control algorithm also has integrated protection against battery overcharging during the stand-alone operation. The considered system has been experimentally tested over wide ranges of irradiance and PV panel temperature.

Keywords: battery; maximum power point; photovoltaic source; small-signal model; transfer functions; quasi-Z-source inverter

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1. Introduction

Solar energy as a clean and fully renewable source of energy can be harnessed all over the world and directly converted to electricity by means of photovoltaic (PV) systems. The main component of these systems is a PV source composed of multiple interconnected PV panels. The PV source produces dc voltage and current, so in the case of the grid-tied operation or the stand-alone operation with ac loads, it is commonly combined with a dc–dc boost converter, to ensure required voltage boost and maximum power production of a PV source, and a voltage-source inverter [1–3]. The alternative is the utilization of a quasi-Z-source inverter (qZSI) [4], which enables both the boost and control of the PV source voltage, thus eliminating the requirement for a dc–dc converter. The qZSI ensures boost of the input voltage by means of an impedance network and the additional shoot-through (ST) switching state, which is achieved by short circuiting one or all of the inverter legs during the zero-switching states of the inverter.

The combination of the PV source and the qZSI has been in the scope of many recent studies. In [5,6], PV systems containing the qZSI in the grid-tied applications are analyzed, where the main tasks of the corresponding control algorithms are to ensure the maximum

power production of the PV source and injection of that power into the grid. The main disadvantage of the mentioned systems is the absence of an energy-storage system, so during the stand-alone operation the PV source power has to be equal to the sum of the output load power and system losses. This means that the maximum power production of the PV source practically may not be achieved and the system has to be turned off if the available PV source power is insufficient. To overcome these disadvantages, batteries have been reportedly installed into the impedance network of the qZSI. This allows an expanded operation range of the system during the grid-tied operation and stand-alone operation and the maximum power production of the PV source during the stand-alone operation. In [7,8], the batteries are connected in parallel with the higher-voltage capacitor in the impedance network, whereas in [9–18] they are connected in parallel with the lower-voltage capacitor. The latter topology is more commonly utilized due to the lower required rated voltage of batteries, which implies lower costs of the system implementation.

In the qZSI-based PV systems with the batteries connected in parallel with the lower-voltage capacitor, the tasks of a control algorithm depend on the operation mode. In [13–15,18], during the grid-tied operation, the maximum power production of the PV source is ensured by the variation of the output qZSI current, whereas the battery current/power is controlled by the variation of the duty cycle (d_0). However, in [11,16], the opposite approach is utilized for the same operation. During the stand-alone operation, the only way to achieve the maximum power production of the PV source is by varying the duty cycle [9,12]. To simplify control system design, control algorithms for the grid-tied and stand-alone operation should preferably have a certain degree of similarity in the sense of shared control loops and features. With this in mind, it seems more reasonable to utilize the duty cycle for control of the PV source power, as in [11,16].

An analysis of the qZSI control algorithm often requires knowledge of the small-signal model of the system. These models were determined in [11,13–15] for the PV systems with the PV panel–qZSI–batteries arrangement identical as in this study. In [13–15], the same small-signal model was utilized to obtain a transfer function from the duty cycle to the battery current, which was required for the system analysis. However, during the analysis of the small-signal model in [13–15], several mistakes that adversely affect the model's accuracy have been detected in the corresponding equations, as explained in Section 3. On the other hand, the small-signal model in [11] was utilized to obtain the transfer function from the duty cycle to the PV source voltage. This model is not derived in detail in this study due to the lack of data in [11], but the accuracy of the resulting transfer function is tested.

The electrical power production of the PV source depends on the solar irradiance level (Z) and the temperature of PV panels (T_{pv}). For each combination of these two parameters, there is an operating point, the so-called maximum power point (MPP), which ensures the maximum power production of the PV source. In the case of the PV systems with the battery-assisted qZSI, the most commonly utilized maximum power point tracking (MPPT) algorithm is the perturb-and-observe (P&O) algorithm [19,20], due to its simplicity. This type of algorithm has been utilized in [13–18], and its implementation requires the measurement of the PV source voltage and current. On the other hand, the MPPT algorithm utilized in [9] tracks the MPP based on the measured values of Z and T_{pv}, whereas in [10] a fixed-duty-cycle method [21] was utilized. However, the implementation of sensors for the measurement of Z and T_{pv} increases the system implementation costs and decreases its reliability, whereas the utilization of the fixed-duty cycle implies higher MPP tracking error than in the case of the P&O method, especially in the case of T_{pv} variations.

This paper presents a control algorithm for the qZSI-based PV system with the batteries connected in parallel with the lower-voltage capacitor in the impedance network. The proposed control algorithm enables both grid-tied and stand-alone operation of the considered system and it is implemented in the d–q synchronous reference frame. During the grid-tied operation, the battery current controller provides the reference value for the d-axis grid current controller, whereas the q-axis reference current equals zero to ensure

unity power factor. During the stand-alone operation, the *d*-axis and *q*-axis load voltage controllers provide the reference values for the corresponding current controllers. The control system design is based on knowledge of three transfer functions which were obtained according to the novel small-signal model of the considered system derived in this study due to the mentioned shortcomings of the existing models proposed in [11,13–15]. The transfer function from the *d*-axis current to the battery current—determined here for the first time for the considered system configuration—is utilized for the design of the battery current control loop for the grid-tied operation. The transfer function from the duty cycle to the PV source voltage is utilized for the design of the PV source voltage control loop. The proposed P&O MPPT algorithm provides the reference PV source voltage. Unlike the conventional P&O MPPT algorithm, the proposed algorithm does not require the measurement of the PV source current. Instead, the battery current is utilized during the stand-alone operation, whereas the reference *d*-axis current is utilized during the grid-tied operation. This does not imply installation of additional sensors because these two currents are anyway required in the control system, regardless of the MPPT algorithm. In this way, the PV source current sensor may be omitted. The tracking period of the proposed P&O algorithm was determined by using the transfer function from the duty cycle to the battery current, in accordance with the longest settling time noted in the corresponding step response. To prevent overcharging of the batteries during the stand-alone operation, the PV source operating point in some cases needs to depart from the MPP. This kind of battery overcharging protection is integrated within the proposed control algorithm. The proposed control strategy was tested experimentally—for both the grid-tied and stand-alone operation—by using the laboratory setup of the considered system.

2. System Configuration

The considered PV system, including the corresponding control algorithm, is shown in Figure 1. The main components of the system are the PV source with the corresponding terminal capacitor C_{in}, the qZSI with the batteries added in parallel with the lower-voltage capacitor C_2, and the three-phase output LCL filter, composed of inductors L_{f1} and L_{f2}, capacitors C_f, and damping resistors R_d.

The control system of the qZSI is implemented in the *d*–*q* synchronous reference frame, with the inverter output voltages defined as follows [22]:

$$\begin{aligned} v_{od} &= v_d - i_d R_f - L_f \frac{di_d}{dt} + \omega L_f i_q \\ v_{oq} &= v_q - i_q R_f - L_f \frac{di_q}{dt} - \omega L_f i_d \end{aligned} \quad (1)$$

where v_{od}, v_{oq} represent the *d* and *q* axis components of the inverter output voltage, respectively; v_d, v_q represent the *d* and *q* axis components of the inverter bridge output voltage, respectively; i_d, i_q represent the *d* and *q* axis components of the inverter output current, respectively; ω is the angular frequency.

A properly selected bandwidth of the inverter output current controller ensures fairly accurate approximation of the LCL filter with the L filter [23], i.e., $L_f = L_{f1} + L_{f2}$, $R_f = R_{f1} + R_{f2}$, where R_{f1} and R_{f2} represent the corresponding parasitic resistances.

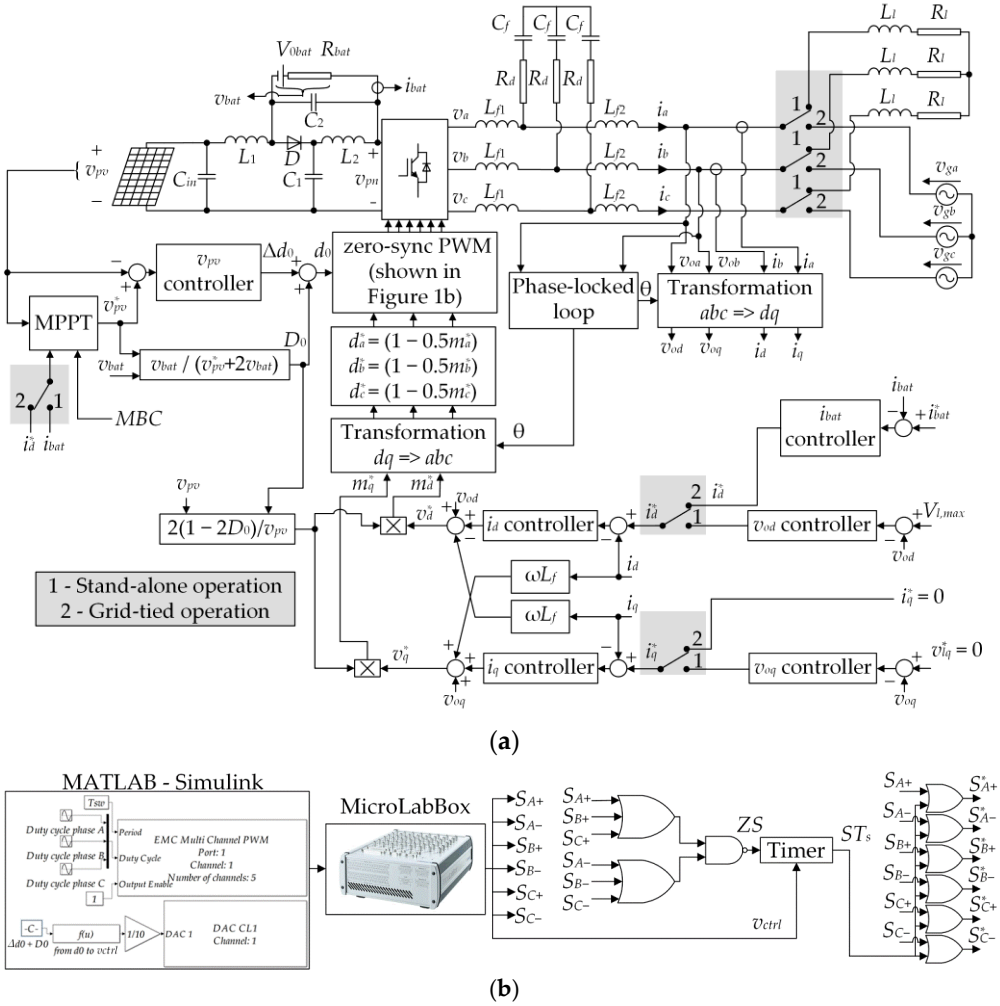


Figure 1. Configuration of the considered system PV system with the qZSI and batteries (**a**), and the logic diagram of the zero-sync PWM (**b**).

2.1. Grid-Tied Operation

During the grid-tied operation, the synchronous reference frame phase-locked loop (PLL) ensures the synchronization of the inverter output voltage with the grid voltage by maintaining $v_{od} = V_{g,max}$ and $v_{oq} = 0$, where $V_{g,max}$ is the amplitude of the grid phase voltage. Note also that, during the grid-tied operation, the system angular frequency is equal to the grid angular frequency, where the angle θ required for the coordinate transformations is obtained as an integral of the angular frequency. The implementation of the PLL ensures the grid active (p_{grid}) and reactive power (q_{grid}) to be defined as follows [22]:

$$\begin{aligned} p_{grid} &= \tfrac{3}{2} i_d V_{g,max} \\ q_{grid} &= -\tfrac{3}{2} i_q V_{g,max} \end{aligned} \tag{2}$$

During the grid-tied operation, the active power injected to the grid is defined by i_d, whereas the reactive power is defined by i_q. The reference d-axis current (i^*_d) is obtained as the output of the battery current controller, whereas the reference q-axis current (i^*_q) is set to zero.

2.2. Stand-Alone Operation

During the stand-alone operation, two controllers are introduced to control voltages v_{od} and v_{oq}. The reference of the d-axis voltage controller (v^*_{od}) is set equal to the amplitude of the phase load voltage ($V_{l,max}$). On the other hand, the reference q-axis voltage (v^*_{oq}) is

set to zero in order to ensure the load active (p_{load}) and reactive power (q_{load}) to be defined as follows [22]:

$$\begin{aligned} p_{load} &= \tfrac{3}{2} i_d V_{l,max} \\ q_{load} &= -\tfrac{3}{2} i_q V_{l,max} \end{aligned} \tag{3}$$

Note that, during the stand-alone operation, the angular frequency obtained by the phase-locked loop amounts to $\omega = 2\pi f_l$, where f_l is the desired fundamental frequency of the load voltage/current (in this study, 50 Hz).

2.3. Maximum Power Point Tracking of the Photovoltaic Source

The I–V characteristics of the PV source are not linear and the electric power generated by the PV source varies with the irradiance and the temperature of the PV panels. However, there is an operating point where the PV source generates maximum power. Therefore, the MPPT algorithm is utilized to ensure the MPP operation of the PV source for different values of the solar irradiance and the PV panel temperature. In the considered system shown in Figure 1a, the proposed P&O MPPT algorithm tracks the MPP with the corresponding tracking period by varying the PV source voltage (v_{pv}). The main advantage of this algorithm is that it does not require the measurement of the PV source current, which allows elimination of the corresponding sensor. During the grid-tied operation, the MPPT algorithm detects the MPP based on v_{pv} and the reference d-axis grid current, whereas during the stand-alone operation it detects the MPP based on v_{pv} and the battery current (i_{bat}). Note that during the stand-alone operation, the battery current is not controlled, so in the case of the fully charged batteries, further charging has to be prevented. For that purpose, the maximum battery charge signal (*MBC* in Figure 1a) is implemented in the control algorithm. The detailed analysis of the proposed MPPT algorithm is given in Section 4.

In this study, the sinusoidal pulse-width modulation (PWM) with injected third harmonic and dead time is implemented [24]. The ST states are injected by means of the zero-sync PWM, proposed and detailed in [24], whose logic diagram is shown in Figure 1b. This method ensures wider range of the duty cycle and lower qZSI losses in comparison to the conventional ST states injection method without dead time.

3. Small-Signal Model of the System

The small-signal model of the considered system is obtained by considering the equivalent circuits of the qZSI in the non-ST state and ST state, which are shown in Figure 2a,b, respectively. R_{L1} and R_{L2} represent the parasitic resistances of the impedance network inductors. Note that the influence of the terminal capacitor C_{in} is neglected, which implies that the PV source current (i_{pv}) equals the qZSI inductor current (i_{L1}). In this paper, a symmetrical impedance network is considered, i.e., $L_1 = L_2 = L$, $C_1 = C_2 = C$, $R_{L1} = R_{L2} = R_L$. During the non-ST state, the impedance network is coupled to the load/grid, which allows the power flow from the PV source and the batteries to the load/grid. In this state, the diode D (Figure 1a) is forward biased, and the capacitors C_1 and C_2 are being charged, whereas the currents through L_1 and L_2 are decreasing. The dynamic state–space equations of the qZSI for the non-ST state, obtained based on Figure 2a, are given as follows:

$$\mathbf{F} d\mathbf{x}/dt = \mathbf{A_{nST}}\mathbf{x} + \mathbf{B_{nST}}\mathbf{u} \tag{4}$$

where

$$\mathbf{x} = \begin{bmatrix} i_{L1} & i_{L2} & v_{C1} & i_{bat} \end{bmatrix}^T, \mathbf{u} = \begin{bmatrix} v_{pv} & i_{pn} & V_{0bat} \end{bmatrix}^T,$$

$$\mathbf{A_{nST}} = \begin{bmatrix} -R_L & 0 & -1 & 0 \\ 0 & -R_L & 0 & R_{bat} \\ 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & -1 \end{bmatrix}, \mathbf{B_{nST}} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & -1 \\ 0 & -1 & 0 \\ 0 & 1 & 0 \end{bmatrix}, \mathbf{F} = \begin{bmatrix} L & 0 & 0 & 0 \\ 0 & L & 0 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & R_{bat}C \end{bmatrix}$$

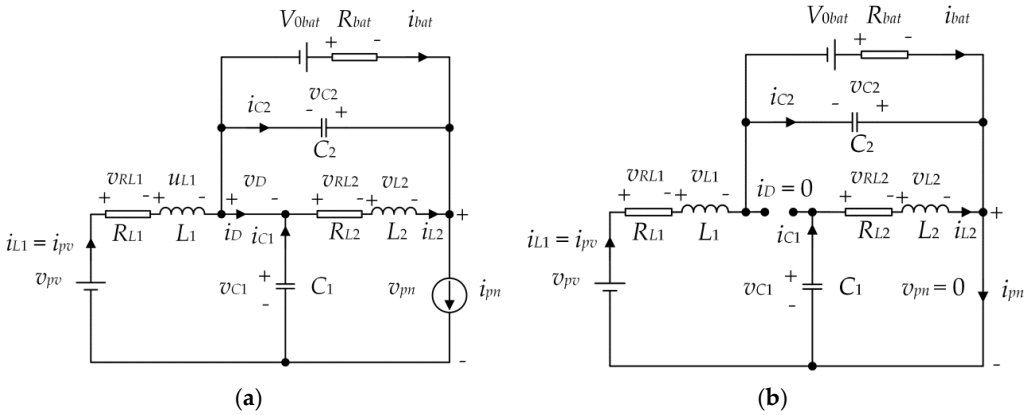


Figure 2. Equivalent circuits of the qZSI: non-ST state (**a**) and ST state (**b**).

The state–space variables are the two inductor currents (i_{L1} and i_{L2}), the voltage across C_1 (v_{C1}), and the battery current (i_{bat}). The input variables of the model are the PV source voltage (v_{pv}), the input current of the inverter bridge (i_{pn}), and the battery open-circuit voltage (V_{0bat}). Finally, the duty cycle (d_0) is defined as T_0/T_{sw}, where T_0 and T_{sw} represent the ST state period and the switching period, respectively, whereas R_{bat} utilized in (4) represents the equivalent resistance of the batteries.

The ST state always occurs only during the zero-switching state, in which the impedance network is practically disconnected from the load/grid. During the ST state, the inverter bridge is short-circuited, which causes blocking of the diode D (Figure 1a), discharging of the capacitors C_1 and C_2, and an increase in i_{L1} and i_{L2}. The utilization of the ST state ensures the boost of the PV source voltage. The dynamic state–space equations of the qZSI for the ST state are obtained, based on Figure 2b, as:

$$\mathbf{F}d\mathbf{x}/dt = \mathbf{A_{ST}x} + \mathbf{B_{ST}u} \tag{5}$$

where

$$\mathbf{A_{ST}} = \begin{bmatrix} -R_L & 0 & 0 & -R_{bat} \\ 0 & -R_L & 1 & 0 \\ 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & -1 \end{bmatrix}, \ \mathbf{B_{ST}} = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix},$$

The system average state–space equations are obtained by using state–space averaging, as follows:

$$\mathbf{F}d\mathbf{x}/dt = \mathbf{Ax} + \mathbf{Bu} \tag{6}$$

where

$$\mathbf{A} = \mathbf{A_{ST}}d_0 + \mathbf{A_{nST}}(1-d_0) = \begin{bmatrix} -R_L & 0 & d_0-1 & -d_0R_{bat} \\ 0 & -R_L & d_0 & (1-d_0)R_{bat} \\ 1-d_0 & -d_0 & 0 & 0 \\ d_0 & d_0-1 & 0 & -1 \end{bmatrix}$$

$$\mathbf{B} = \mathbf{B_{ST}}d_0 + \mathbf{B_{nST}}(1-d_0) = \begin{bmatrix} 1 & 0 & d_0 \\ 0 & 0 & d_0-1 \\ 0 & d_0-1 & 0 \\ 0 & 1-d_0 & 0 \end{bmatrix}$$

The dynamic small-signal model of the considered system is obtained from the average state–space equations by utilizing the small-perturbation method and Laplace transforma-

tion. The I–V characteristic of the PV source may be described in the Laplace domain by utilizing the equivalent PV source resistance (R_{fn}), as follows [5,6]:

$$\widetilde{v}_{pv}(s) = -R_{fn}\widetilde{i}_{L1}(s) \tag{7}$$

Finally, the average state–space equations in the Laplace domain, with the considered perturbation of the PV source voltage as per (7), are given as follows:

$$(R_L + sL)\widetilde{i}_{L1}(s) = (D_0 - 1)\widetilde{v}_{C1}(s) - R_{bat}D_0\widetilde{i}_{bat}(s) - R_{fn}\widetilde{i}_{L1}(s) + D_0\widetilde{v}_{0bat} + \widetilde{d}_0(s)V_{11} \tag{8}$$

$$(R_L + sL)\widetilde{i}_{L2}(s) = D_0\widetilde{v}_{C1}(s) + (1 - D_0)R_{bat}\widetilde{i}_{bat}(s) + (D_0 - 1)\widetilde{v}_{0bat} + \widetilde{d}_0(s)V_{11} \tag{9}$$

$$Cs\widetilde{v}_{C1}(s) = (1 - D_0)\widetilde{i}_{L1}(s) - D_0\widetilde{i}_{L2}(s) + (D_0 - 1)\widetilde{i}_{pn}(s) + \widetilde{d}_0(s)I_{11} \tag{10}$$

$$CsR_{bat}\widetilde{i}_{bat}(s) = D_0\widetilde{i}_{L1}(s) + (D_0 - 1)\widetilde{i}_{L2}(s) - \widetilde{i}_{bat}(s) + (1 - D_0)\widetilde{i}_{pn}(s) - \widetilde{d}_0(s)I_{11} \tag{11}$$

In (7)–(11), capital letters represent the steady-state values of the considered variables, $V_{11} = V_{C1} - I_{bat}R_{bat} + V_{0bat}$, $I_{11} = I_{bat} - 2I_{L1} + I_{pn}$, whereas "~" denotes the variables obtained as the Laplace transform of the corresponding perturbation (e.g., $\widetilde{d}_0$ is equal to the Laplace transform of Δd_0).

Equations (8)–(11) are used to obtain transfer functions which may be used for control system design. The first transfer function from the duty cycle to the PV source voltage is obtained from (8)–(11). However, the transfer functions from the duty cycle to the battery current and from the *d*-axis grid current to the battery current require one more equation. In the non-ST state, this equation is defined as:

$$i_{pn}V_{pn} = \frac{3}{2}v_{od}i_d \tag{12}$$

where V_{pn} represents the peak value of the inverter bridge input voltage of the ideal qZSI.

In (12), the input power of the inverter bridge is assumed equal to the inverter output power expressed in the *d*–*q* coordinate system, which implies neglecting of the inverter bridge losses and output LCL filter losses.

In the ST state, there is no exchange of energy between the ac and dc sides of the inverter bridge. Consequently, the average equation is obtained by multiplying the inverter input power during the non-ST state (left side of (12)) with the factor $(1 - d_0)$, as follows:

$$i_{pn}V_{pn}(1 - d_0) = \frac{3}{2}v_{od}i_d \tag{13}$$

In (13), v_{od} may be obtained as a function of V_{pn} and the amplitude modulation index (m_a), as follows:

$$v_{od} = \frac{V_{pn}}{2}m_a \tag{14}$$

With respect to (14), (13) becomes:

$$i_{pn}(1 - d_0) = \frac{3}{4}m_a i_d \tag{15}$$

By utilizing the small-perturbation method and Laplace transformation, (15) becomes:

$$\widetilde{i}_{pn}(s)(1 - D_0) - \widetilde{d}_0(s)I_{pn} = \frac{3}{4}\widetilde{m}_a(s)I_d + \frac{3}{4}M_a\widetilde{i}_d(s) \tag{16}$$

where capital letters represent the steady-state values of the considered variables.

The transfer function from the *d*-axis grid current to the battery current is obtained based on (8)–(11) and (16). In the five considered equations, there are nine variables, so in order to obtain the desired transfer function, the perturbances of three variables should be set to zero. It is assumed that, during the perturbation of the *d*-axis grid current, the

modulation index, the open-circuit voltage of the batteries, and the duty cycle remain constant. Finally, with $\widetilde{m}_a(s) = 0$, $\widetilde{v}_{0bat}(s) = 0$, and $\widetilde{d}_0(s) = 0$, the transfer function from the d-axis grid current to the battery current is given as follows:

$$G_{\widetilde{i}_d}^{\widetilde{i}_{bat}} = \frac{1}{4}\frac{N_3 s^3 + N_2 s^2 + N_1 s + N_0}{K_4 s^4 + K_3 s^3 + K_2 s^2 + K_1 s + K_0} \tag{17}$$

where

$$N_0 = 3M_a R_L + 3D_0 M_a R_{fn},\ N_1 = 3M_a L + 3CM_a R_L^2 + 3CM_a R_{fn} R_L,$$

$$N_2 = 6CM_a L R_L + 3CM_a R_{fn} L,\ N_3 = 3CM_a L^2,$$

$$K_0 = 2D_0^2 R_L + 4D_0^2 R_{bat} + D_0^2 R_{fn} - 2D_0 R_L - 4D_0 R_{bat} + R_L + R_{bat}$$

$$K_1 = L - 2D_0 L + 2D_0^2 L + CR_L^2 + 2CR_L R_{bat} + CR_L R_{fn} + CR_{bat} R_{fn} + 4CD_0^2 R_L R_{bat} + 2CD_0^2 R_{bat} R_{fn} - -4CD_0 R_L R_{bat} - 2CD_0 R_{bat} R_{fn}$$

$$K_2 = 2CLR_L + 2CLR_{bat} + CLR_{fn} + C^2 R_L^2 R_{bat} - 4CD_0 LR_{bat} + 4CD_0^2 LR_{bat} + C^2 R_L R_{bat} R_{fn}$$

$$K_3 = CL^2 + 2C^2 LR_L R_{bat} + C^2 LR_{bat} R_{fn},\ K_4 = C^2 L^2 R_{bat}.$$

The transfer function obtained in (17) is required for the design of the battery current control loop utilized during the grid-tied operation. On the other hand, the transfer function from the duty cycle to the battery current was obtained from (8)–(11) and (16), by considering the assumptions $\widetilde{v}_{0bat}(s) = 0$, $\widetilde{m}_a(s) = 0$, $\widetilde{i}_d(s) = 0$, as follows:

$$G_{\widetilde{d}_0}^{\widetilde{i}_{bat}} = \frac{1}{4}\frac{P_3 s^3 + P_2 s^2 + P_1 s + P_0}{K_4 s^4 + K_3 s^3 + K_2 s^2 + K_1 s + K_0} \tag{18}$$

where

$$P_0 = -4V_{11} + 8D_0 V_{11} - 4I_{11} R_L + 4I_{pn} R_L - 4D_0 I_{11} R_{fn} + 4D_0 I_{pn} R_{fn},$$

$$P_1 = -4I_{11} L + 4I_{pn} L - 4CR_L V_{11} - 4CR_{fn} V_{11} - 4CI_{11} R_L^2 + 4CI_{pn} R_L^2 + +8CD_0 R_L V_{11} + 4CD_0 R_{fn} V_{11} - 4CI_{11} R_L R_{fn} + 4CI_{pn} R_L R_{fn}$$

$$P_2 = -4CLV_{11} + 8CD_0 LV_{11} - 8CI_{11} LR_L - 4CI_{11} LR_{fn} + 8CI_{pn} LR_L + 4CI_{pn} LR_{fn},$$

$$P_3 = -4CI_{11} L^2 + 4CI_{pn} L^2$$

The transfer function given in (18) was utilized only for the selection of the MPPT algorithm tracking period (T_{mppt}) because the longest settling time of the battery current response is noted for step changes in the duty cycle. Note that the transfer function from the duty cycle to the battery current has been already derived in [13–15], but errors have been detected in the corresponding small-signal model. First, in the system of Equation (5) in [14], $(1–d_0)V_{0bat}$ in the second equation should be replaced by $(d_0-1)V_{0bat}$. The second detected error is the utilization of an equation that defines the steady-state battery current for the determination of the dynamic model of the system.

The transfer function from d_0 to v_{pv} is obtained from (8)–(11), by considering the assumptions $\widetilde{i}_{bat}(s) = 0$ and $\widetilde{v}_{0bat}(s) = 0$. This transfer function is required for the design of the PV source voltage control loop for both the grid-tide and stand-alone operation, and it is expressed as follows:

$$G_{\widetilde{d}_0}^{\widetilde{v}_{pv}} = -R_{fn} G_{\widetilde{d}_0}^{\widetilde{i}_{L1}} = -R_{fn}\frac{CLV_{11}s^2 + CR_L V_{11} s + V_{11}}{CL^2 s^3 + (2CLR_L + CR_{fn} L)s^2 + (L + CR_L^2 + CR_{fn} R_L)s + R_L + D_0 R_{fn}} \tag{19}$$

The steady-state values of the state–space variables are obtained from (6), by setting the right side equal to zero, as follows:

$$\begin{aligned} I_{L1} &= \frac{-d_0 I_{bat} - (d_0 - 1) I_{pn}}{1 - 2d_0} \\ I_{L2} &= \frac{(d_0 - 1) I_{bat} - (d_0 - 1) I_{pn}}{1 - 2d_0} \\ I_{L1} - I_{L2} &= I_{bat} \\ V_{C1} &= \frac{1 - d_0}{1 - 2d_0} V_{pn} + \frac{2d_0(1 - d_0) R_L I_{bat} - (1 - d_0) R_L I_{pn}}{(1 - 2d_0)^2} \\ V_{C2} &= \frac{d_0}{1 - 2d_0} V_{pn} + \frac{\left(2d_0^2 - 2d_0 + 1\right) R_L I_{bat} + (d_0 - 1) R_L I_{pn}}{(1 - 2d_0)^2} \end{aligned} \tag{20}$$

In the case $R_L = 0$, the expressions for the voltages V_{C1} and V_{C2} obtained from (20) are equal to the expressions well-known from the literature [4]. The steady-state values obtained in (20) differ from those obtained in [13–15] due to the above-described errors in the corresponding small-signal model.

4. Control Schemes for the Grid-Tied Operation and Stand-Alone Operation

The control algorithm of the considered PV system deals with multiple tasks. During the grid-tied operation, the battery current is controlled through the adjustment of the reference *d*-axis grid current. On the other hand, during the stand-alone operation, the *d* and *q* axis components of the load voltage are controlled through the adjustment of the corresponding reference *d* and *q* axis currents, respectively. In both the considered cases, the PV source power is controlled through the adjustment of the PV source voltage. The detailed analysis of the respective control loops is given below.

4.1. Control of the Battery Current for the Grid-Tied Operation

The battery current control loop is shown in Figure 3. The output value of the battery current controller is the reference *d*-axis grid current (i^*_d), which practically means that the battery controller controls the active power injected to the grid. The inner control loop—highlighted in grey in Figure 3—contains the *d*-axis current controller and the transfer function of the output filter, with neglected dynamics of the inverter bridge. Note that the output filter was modeled as an *L* filter ($L_f = L_{f1} + L_{f2}$, $R_f = R_{f1} + R_{f2}$) since the properly selected bandwidth of the *d*-axis current controller ensures fairly accurate approximation of the LCL filter with the L filter [23]. The transfer function from the *d*-axis grid current to the battery current given in (17) was utilized to obtain the battery current, which is then filtered by the first order filter in the feedback loop.

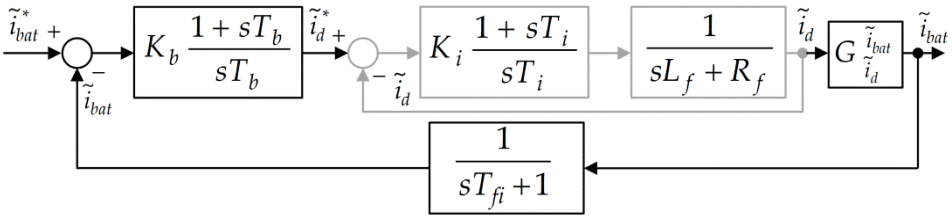


Figure 3. Battery current control loop.

The *q*-axis grid current control loop is identical to the inner control loop shown in Figure 3, including the values of the controller parameters, with the corresponding reference value (i^*_q) set to zero to ensure zero reactive power.

4.2. Control of the Inverter Output Voltage for the Stand-Alone Operation

Figure 4 shows the control loop of the *d*-axis load voltage (v_{od}) during the stand-alone operation. The reference *d*-axis voltage (v^*_{od}) defines the amplitude of the phase load voltage since the reference *q*-axis voltage (v^*_{oq}) is set to zero, as shown in Figure 1a. The output value of the voltage controller in Figure 4 is the reference *d*-axis load current.

The corresponding inner loop in Figure 4 is the same as that for the grid-tied operation (Figure 3), including the values of the current controller parameters. The transfer function of the load is utilized to obtain v_{od} from i_d. The load is modeled as a resistive–inductive load with the corresponding inductance L_l and the resistance R_l.

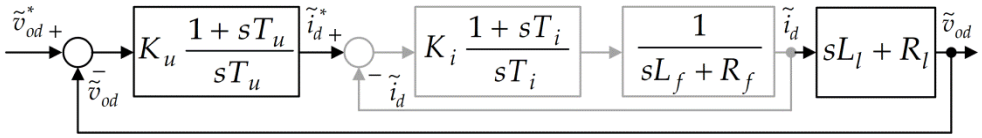


Figure 4. Control loop of the *d*-axis load voltage.

The same control loop as in Figure 4 is utilized for the load *q*-axis voltage during the stand-alone operation, including the values of the controllers' parameters. Due to the fact that v^*_{oq} equals zero, the reference *q*-axis current (i^*_q) defines the reactive power required by the load. This means that, in the case of the resistive load, the *q*-axis current will be equal to zero, whereas in the case of the resistive–inductive load, this current will be negative.

4.3. Control of the Photovoltaic Source Voltage and Maximum Power Point Tracking

The control loop of the PV source voltage is shown in Figure 5. The reference PV source voltage (v^*_{pv}) is provided by the MPPT algorithm, whereas the output signal of the respective voltage controller is the duty cycle. The transfer function from the duty cycle to the PV source voltage, given in (19), is utilized to obtain the PV source voltage based on the duty cycle. The control scheme shown in Figure 5 is utilized for the tuning of the PV source voltage controller.

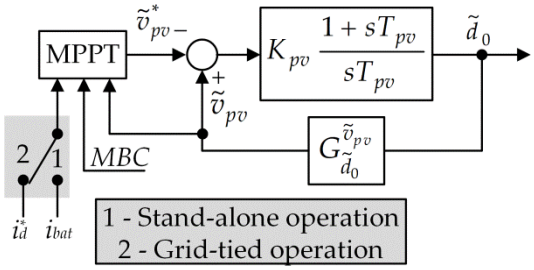


Figure 5. Control loop of the PV source voltage.

As shown in Figure 5, the PV source voltage is controlled by varying the duty cycle, which is enabled by connecting the batteries in parallel with C_2, yielding [4]:

$$V_{bat} = V_{C2} = \frac{d_0}{1-2d_0} V_{pv} \tag{21}$$

where the mean values of the considered variables are denoted by capital letters.

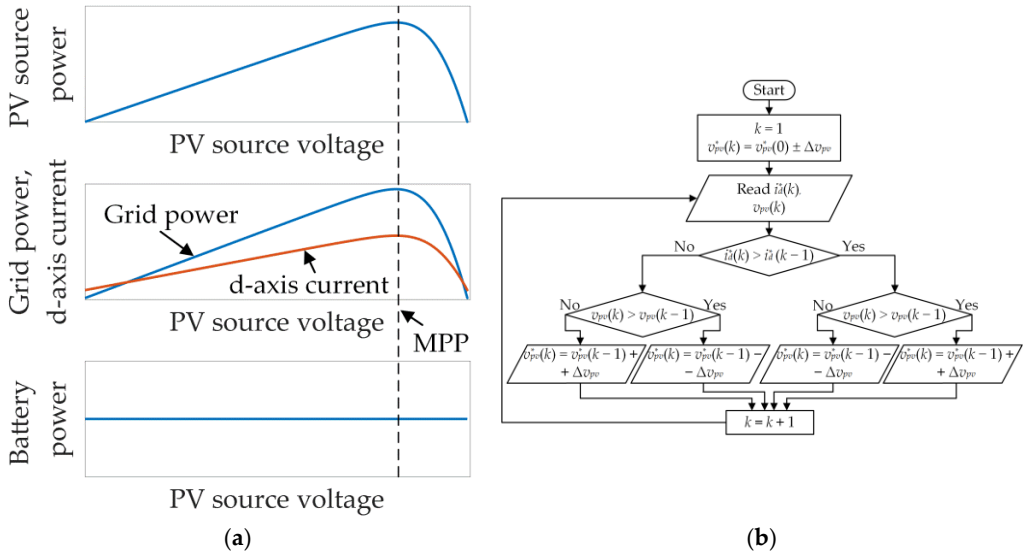
The battery voltage (V_{bat}) is approximately constant, so the variation of the duty cycle (d_0) results in the variation of V_{pv}. The equivalent duty cycle is obtained as the sum of the duty cycle obtained by the controller and the corresponding feed-forward signal (D_0) obtained according to (21) as $V_{bat}/(V^*_{pv} + 2V_{bat})$.

In the conventional P&O MPPT algorithm, the MPP is achieved by considering the PV source voltage and power, which requires the measurement of the PV source voltage and current. The P&O MPPT algorithm proposed in this study requires the PV source voltage and the reference *d*-axis grid current during the grid-tied operation, whereas it requires the PV source voltage and the battery current during the stand-alone operation. In this way, the PV source current sensor is omitted. In addition, the currents i^*_d and i_{bat} are required by the control algorithm, regardless of the MPPT algorithm. This means

that the number of required sensors in the system is reduced by one. Note also that the *MBC* signal is implemented in the control algorithm in order to disable charging of the already fully charged batteries during the stand-alone mode. In the case of *MBC* = 0, battery charging is enabled and the system operates in the MPP, whereas in the case of *MBC* = 1, the battery current is limited to values higher than or equal to zero to prevent further charging. Therefore, the system operating point may depart from the MPP in the case of *MBC* = 1.

Figure 6a shows the PV source power (p_{pv}), the grid power (p_{grid}), the *d*-axis grid current, and the battery power (p_{bat}) during the grid-tied operation. In this case, the battery current is considered constant since the battery current reference is set to a constant value. The power relation during the grid-tied operation with omitted power losses is defined as follows:

$$\begin{aligned} p_{pv} + p_{bat} &= p_{grid} \\ v_{pv} i_{pv} + i_{bat} v_{bat} &= \tfrac{3}{2} V_{g,max} i_d \end{aligned} \tag{22}$$



(**a**) (**b**)

Figure 6. Grid-tied operation: PV source power, grid power and *d*-axis current, and battery power (**a**), and flow chart of the MPPT algorithm (**b**).

The constant battery power means that the variation of the grid injected power follows the variation of the PV source power (the power losses may also be assumed to change proportionally to the PV source power). Hence, the variation of p_{grid} with v_{pv} is the same as the variation of p_{pv} with v_{pv}, as shown in Figure 6a. The MPP of the PV source power corresponds to the MPP of the grid injected power, so p_{pv} may be replaced by p_{grid} in the MPPT algorithm. Finally, p_{grid} may be replaced by the reference *d*-axis grid current since the grid voltage is considered constant ($V_{g.max}$ = const.). Note that the system is robust to a grid voltage sag, since T_{mppt} amounts to a few hundred ms. Figure 6b shows the flow chart of the MPPT algorithm during the grid-tied operation. As compared to the conventional P&O algorithm, the PV source power is here replaced by the reference *d*-axis grid current.

Figure 7a shows the PV source power (p_{pv}), the load power (p_{load}), the battery power (p_{bat}), and the battery current during the stand-alone operation. In this case, the load power is considered to be slowly varying in comparison with the PV source dynamics, so it may be regarded as constant during the PV source power variation. The power balance equation for the stand-alone operation with omitted power losses is defined as follows:

$$\begin{aligned} p_{pv} &= p_{load} - p_{bat} \\ v_{pv} i_{pv} &= \tfrac{3}{2} V_{l,max} i_d - i_{bat} v_{bat} \end{aligned} \tag{23}$$

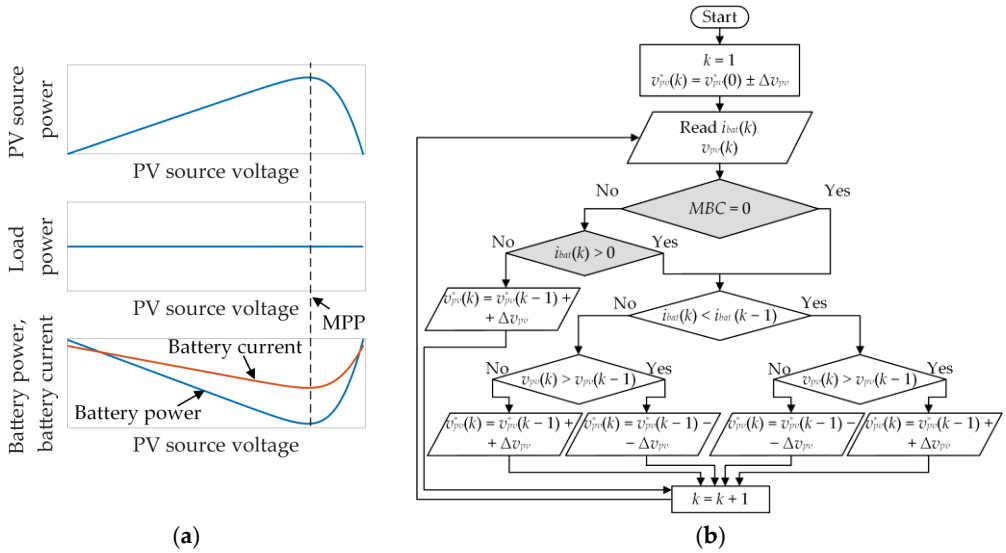


Figure 7. Stand-alone operation: PV source power, load power, and battery power and current (**a**), and flow chart of the PV source reference voltage determination (**b**).

The constant load power means that the variation of the battery power follows the variation of the PV source power. During battery discharge, the battery power decreases with the increase in the PV source power, whereas during charging, although its absolute value increases with the increase in the PV source power, the battery power changes sign and actually continues to decrease in value. Therefore, in both considered battery modes, the maximum PV source power corresponds to the minimum battery current, as shown in Figure 7a. Consequently, during the stand-alone operation, the PV source power may be replaced by the battery power in the MPPT algorithm. Finally, the battery power may be replaced by the battery current provided that the battery voltage is considered as approximately constant.

Figure 7b shows the flow chart utilized for the determination of the PV source reference voltage (v^*_{pv}) during the stand-alone operation, which consists of two parts. The first part is the proposed P&O algorithm, where the PV source power is replaced with the battery current. The second part encompasses conditions added to prevent overcharge of the batteries, which are grey colored in Figure 7b. In the case when the battery charging is allowed, the *MBC* value equals 0 and v^*_{pv} is set to achieve the MPP. However, in the case when the batteries are fully charged, the *MBC* value equals 1 and v^*_{pv} is set to ensure that the battery current does not drop below zero, thus preventing further charging. In the case when *MBC* = 1 and the battery current is negative, the reference PV source voltage is increased, which, in turn, causes the decrease in the PV source power (i.e., the new PV source operating point is placed right of the MPP on the I–V (or P–V) characteristics of the PV source). The battery current eventually oscillates at around zero. The corresponding mean value may slightly differ from zero, but this error is practically negligible and it may be further reduced by decreasing the variation step of v^*_{pv} (Δv_{pv}). Note that the PV source power could be alternatively decreased by decreasing the reference voltage (i.e., by placing the operating point left of the MPP). However, the first-mentioned approach results in lower current ripple and power losses and was, hence, utilized in this study.

5. Experimental Implementation of the System

5.1. Laboratory Setup

Figure 8 shows the laboratory setup of the considered PV system. The main components are denoted as follows:

1. DC power supply Chroma 62050H 600S, programmed to emulate 16 series-connected PV panels KC200GT (Kyocera).

2. Hall-effect transducers LA 55-P/SP52 [25] (for the battery current and the grid/load phase currents), DVL 500 [26] (for the PV source voltage), CV 3–500 [27] (for the grid voltages), and LV 25-P (for the load voltages) (LEM).
3. qZSI impedance network with $L_1 = L_2 = 20.2$ mH (unsaturated), $R_L = 0.5\ \Omega$ (at 25 °C)), and $C_1 = C_2 = 50\ \mu$F (ESR = 7.8 mΩ).
4. qZSI three-phase inverter bridge (IXBX75N170 IGBTs (IXYS) and SKHI 22B(R) drivers (Semikron)).
5. LCL filter at the qZSI output stage ($L_{f1} = 8.64$ mH, $L_{f2} = 4.32$ mH, $R_{f1} = 0.1036\ \Omega$, $R_{f2} = 0.0518\ \Omega$, $C_f = 4\ \mu$F, $R_d = 10\ \Omega$), with the design details given in Appendix A.
6. MicroLabBox controller board (dSpace) for the qZSI control.
7. A symmetric three-phase resistive load.
8. The battery system composed of 22 lead-acid batteries connected in series with a total open-circuit voltage amounting to about 270 V.

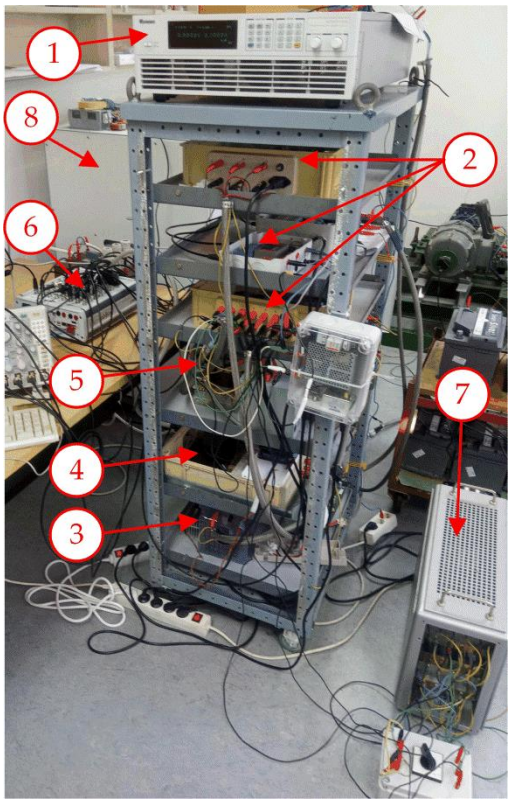


Figure 8. Laboratory setup of the qZSI with the PV source and batteries.

The major part of the control algorithm was executed with the sampling frequency of 10 kHz. Exceptions are the MPPT algorithm—executed with 5 Hz—and the battery current sampling and filtering—executed with 20 kHz—with the time constant of the corresponding first-order filter (T_{fi}) set to 5 ms. In this way, the steady-state error of the measured battery current—that otherwise exists when the battery current waveform is sampled with lower frequencies—is eliminated. The sampling frequency of the MPPT algorithm ($f_{mppt} = 1/T_{mppt}$) was chosen so as to ensure that all the corresponding transients disappear within a single sampling interval. Note that f_{mppt} has to be a multiple of the sampling frequencies of 10 kHz and 20 kHz due to the multitask operation of MicroLabBox.

The synchronous reference frame PLL with the moving average filter (MAF) [28] was utilized in this study during the grid-tied operation. The corresponding controller parameters have been set to $K_{pll} = 0.0464$ rad/Vs and $T_{pll} = 0.02$ s, whereas the MAF widow was set to 0.01 s in order to completely remove the 100 Hz harmonics and all its multiples from the filtered v_{oq} [29].

The duty cycle (d_0) is converted into the control voltage (v_{ctrl}) of the LM555CN timer, which results in the desired T_0 (Figure 1b). The equation that defines v_{ctrl} according to d_0 is given as follows [24]:

$$v_{ctrl} = V_{cc}\left(1 - e^{-\frac{d_0 T_{sw}/2}{T_t}}\right) = V_{cc}\left(1 - e^{-\frac{T_0/2}{T_t}}\right) \quad (24)$$

where V_{cc} represents the supply voltage of the timer (5 V in this study), T_t represents the corresponding time constant (20.8 µs in this study), and T_{sw} is set to 0.2 ms in this study.

5.2. Accuracy Verification of the Proposed Transfer Functions

The accuracy verification of the proposed transfer functions was carried out by comparison of the waveforms calculated by means of the transfer function with those obtained by measurement. Figure 9a shows the setup utilized for the verification of the transfer function from i_d to i_{bat}. The input signal of the transfer function is the measured waveform of i_d, whereas the output signal denoted as i_{bat} is the calculated battery current, which is then filtered with the same first-order filter as the measured battery current ($i_{bat\text{-}measured}$). Finally, the filtered calculated battery current denoted as $i_{bat/id\text{-}tf}$ is compared with the filtered measured battery current. Note that all the measurements for the verification of the transfer function from i_d to i_{bat} were carried out during the grid-tied operation for the constant PV source power.

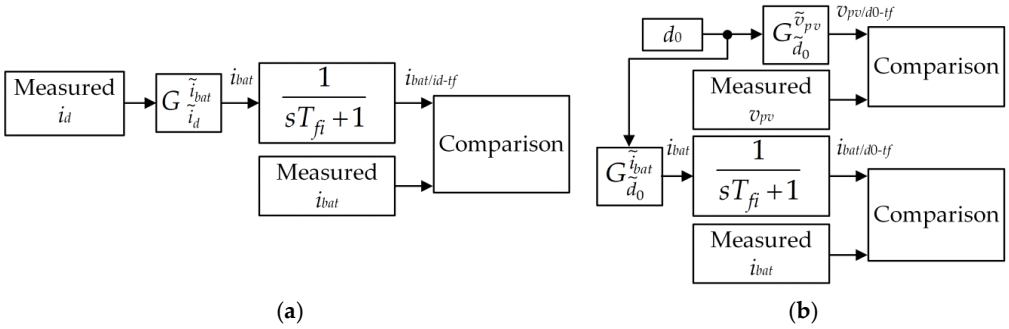


Figure 9. Setups utilized for the accuracy verification of transfer functions: from *d*-axis gird current to battery current (**a**), and from duty cycle to battery current/ PV source voltage (**b**).

Figure 9b shows the setup utilized for the verification of the transfer functions from d_0 to i_{bat} and from d_0 to v_{pv}. The input signal for both the considered transfer functions—the duty cycle (d_0)—is determined by the control algorithm. The output signal of the transfer function from d_0 to v_{pv} ($v_{pv/d0\text{-}tf}$) is compared with the measured v_{pv} ($v_{pv\text{-}measured}$), whereas the filtered output signal of the transfer function from d_0 to i_{bat} ($i_{bat/d0\text{-}tf}$) is compared with the filtered measured battery current $i_{bat\text{-}measured}$. These two transfer functions were tested during the stand-alone operation for the constant load power.

The accuracy verification of the transfer function from i_d to i_{bat} was carried out for three different combinations of the irradiance value (Z) and the PV panels' temperature (T_{pv}). The linearization of the considered transfer function was carried out for Z = 600 W/m^2 and T_{pv} = 30 °C. These values represent the approximate average values of Z and T_{pv} encompassed in the measurements in this study (i.e., Z is varied from 300 W/m^2 to 1000 W/m^2, whereas T_{pv} is varied from 10 °C to 50 °C). The linearization was carried out in the MPP, where the input parameters of the transfer function from i_d to i_{bat}, defined in (17), are given in Table 1.

Table 1. The input parameters of the transfer function from i_d to i_{bat}.

R_{bat} (Ω)	R_{fn} (Ω)	R_L (Ω)	I_{bat} (A)	I_{L1} (A)	D_0	V_{0bat} (V)	V_{C1} (V)	M_a
0.7	87	0.5	0	4.5	0.284	268	679	0.72

The value of R_{fn} is obtained for the considered operating point based on the corresponding I–V characteristic of the PV source, whereas the R_{bat} value corresponds to the internal resistance of 22 lead-acid batteries connected in series.

Figure 10 shows the comparison of $i_{bat\text{-}measured}$ and $i_{bat/id\text{-}tf}$ for the step variations of i^*_d of ±2 A in three different operating points. First, the i_d value was varied in the linearization point (Z = 600 W/m^2, T_{pv} = 30 °C) and the corresponding waveforms are shown in Figure 10a. The maximum steady-state error in this case amounts to 4%. The transfer function accuracy was also tested for two operating points different than the linearization point. The waveforms shown in Figure 10b were recorded for Z = 1000 W/m^2 and T_{pv} = 10 °C, and the waveforms shown in Figure 10c were recorded for Z = 500 W/m^2 and T_{pv} = 50 °C. The maximum steady-state error in Figure 10b,c amounts to 10.5% and 8%, respectively.

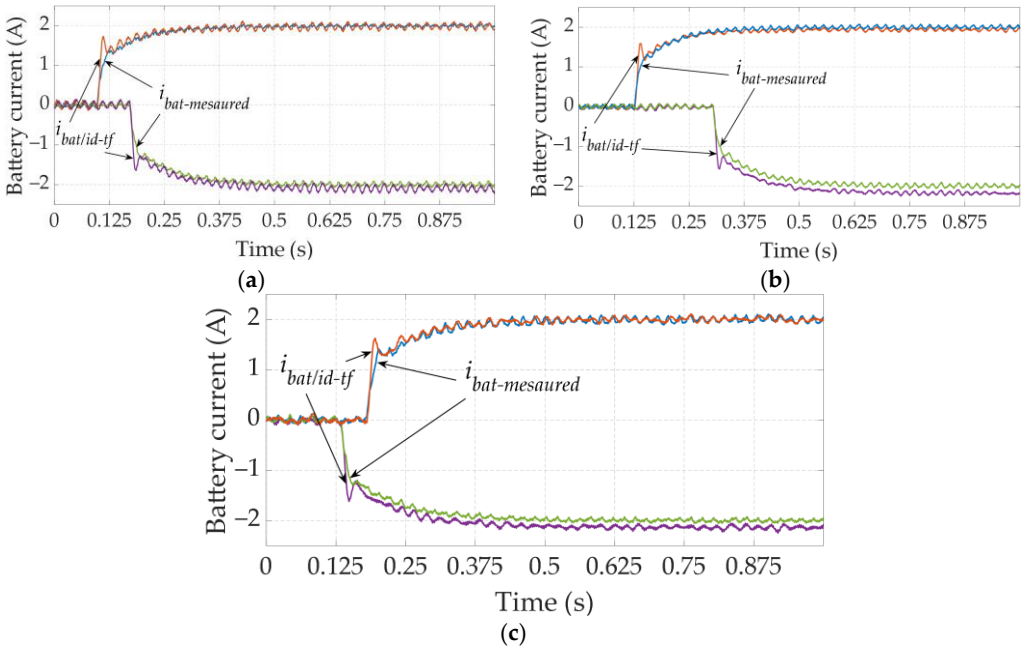


Figure 10. Waveforms of the battery current obtained by the transfer function and by measurement during transients for: Z = 600 W/m^2, T_{pv} = 30 °C (linearization point) (**a**), Z = 1000 W/m^2, T_{pv} = 10 °C (**b**), and Z = 500 W/m^2, T_{pv} = 50 °C (**c**).

The accuracy verification of the transfer functions from d_0 to i_{bat} and from d_0 to v_{pv}—(18) and (19), respectively—was carried out for three values of T_{pv} and with Z set to 600 W/m^2. The linearization of these two transfer functions was carried out in the MPP, with the input parameters given in Table 2.

Table 2. The input parameters of the transfer functions from d_0 to i_{bat} and from d_0 to v_{pv}.

R_{bat} (Ω)	R_{fn} (Ω)	R_L (Ω)	I_{bat} (A)	I_{L1} (A)	D_0	V_{0bat} (V)	V_{C1} (V)	M_a
0.7	87	0.5	1.15	4.5	0.283	270	672	0.73

Figure 11 shows the comparison of $v_{pv\text{-}measured}$ and $v_{pv/d0\text{-}tf}$ for the step variations of d_0 of ± 0.011, for three different operation points. First, the variation of d_0 was carried out in the linearization point (Z = 600 W/m^2, T_{pv} = 30 °C) and the corresponding waveforms are shown in Figure 11a. The maximum steady-state error in this case amounts to 1.6%. In the case of T_{pv} = 10 °C and T_{pv} = 50 °C, waveforms shown in Figure 11b,c, respectively, the maximum steady state error amounts to 2.5% and 4.3%, respectively.

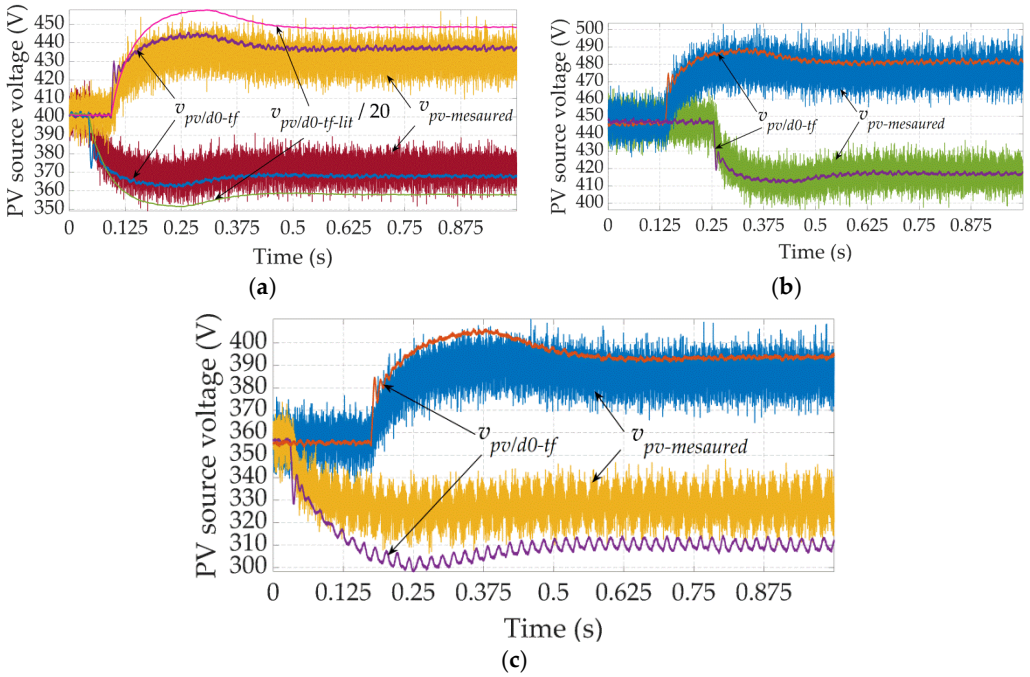


Figure 11. Waveforms of the PV voltage obtained by the transfer function and by measurement during transients for: Z = 600 W/m^2, T_{pv} = 30 °C (linearization point) (**a**), Z = 600 W/m^2, T_{pv} = 10 °C (**b**), and Z = 600 W/m^2, T_{pv} = 50 °C (**c**).

In Figure 11a, waveforms denoted as $v_{pv/d0\text{-}tf\text{-}lit}$ were obtained by the utilizing the transfer function taken from the literature [11], with the input parameters taken from Table 2. Note that $v_{pv/d0\text{-}tf\text{-}lit}$ had to be reduced 20 times in order to fall within the range in Figure 11a. This huge error in the obtained result suggests that the transfer function reported in [11] probably contains one or more overlooked errors.

Figure 12 shows the comparison of $i_{bat\text{-}measured}$ and $i_{bat/d0\text{-}tf}$ for the step variation of d_0 of -0.011, for three different operation points. The lowest maximum steady-state error of approximately 4% is noted for the linearization point shown in Figure 12a (Z = 600 W/m^2, T_{pv} = 30 °C). In the case of T_{pv} = 10 °C and T_{pv} = 50 °C with Z = 600 W/m^2—waveforms shown in Figure 12b,c, respectively—this error amounts to approximately 12%. It is assumed this error is a consequence of the variation of m_a and i_{pn} with the duty cycle, whereas the transfer function defined in (18) is derived with both m_a and i_{pn} considered as constant. However, the transfer function from d_0 to i_{bat} is only utilized for the determination of the MPPT algorithm tracking period (T_{mppt}). Therefore, the estimation of the steady-state value by the considered transfer function is not as important as the estimation of the settling time. Figure 12 shows that the settling time of $i_{bat/d0\text{-}tf}$ is approximately the same as the settling time of $i_{bat\text{-}measured}$ for all the considered operation points. This approves the utilization of the transfer function from d_0 to i_{bat} for the determination of T_{mppt}, since the longest settling time of the battery current response is noted for step changes in the duty cycle.

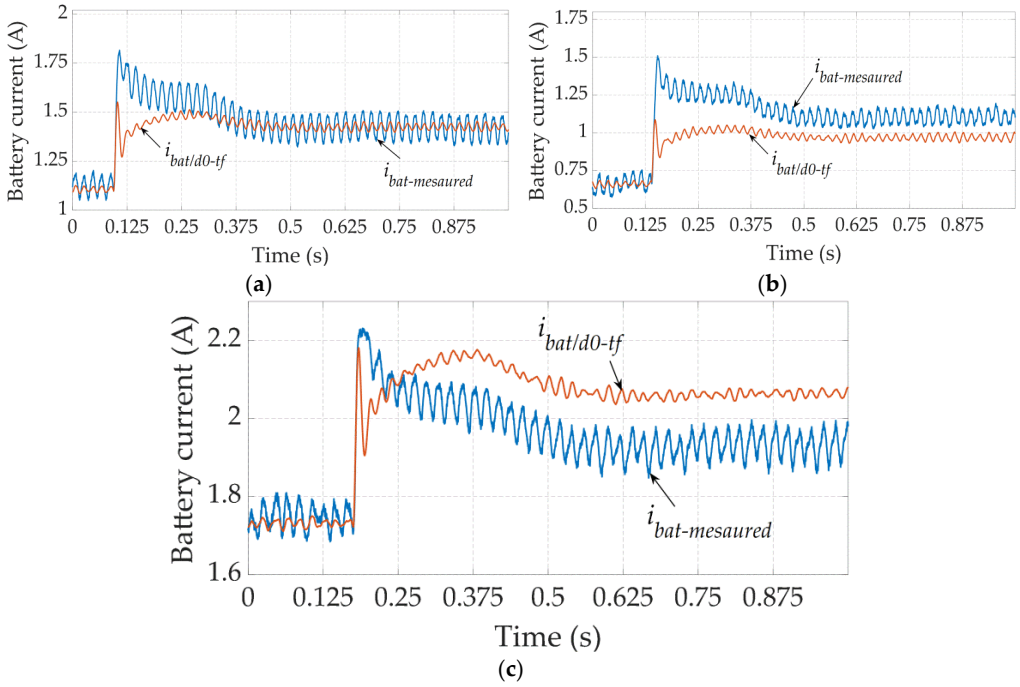


Figure 12. Waveforms of the battery current obtained by the transfer function and by measurement during transients for: Z = 600 W/m^2, T_{pv} = 30 °C (linearization point) (**a**), Z = 600 W/m^2, T_{pv} = 10 °C (**b**), and Z = 600 W/m^2, T_{pv} = 50 °C (**c**).

5.3. Tuning of the PI Controllers

The high noted accuracy of the transfer functions from i_d to i_{bat} and from d_0 to v_{pv} allows the control loops shown in Section 4 to be utilized for the tuning of the system controllers. The *d*- and *q*-axis current controllers in the inner loops in Figures 3 and 4, respectively, were tuned according to the recommendation in [22]. However, it was important to ensure the bandwidth of these current loops to be lower than the resonant frequency of the LCL filter, which is defined as follows [23]:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_{f1}+L_{f2}}{C_f L_{f1} L_{f2}}} = 1200 \text{ Hz} \tag{25}$$

The parameters of i_d and i_q PI controllers are calculated as follows:

$$\begin{aligned} K_i &= \frac{L_{f1}+L_{f2}}{\tau_i} = \frac{0.01296}{0.0005} = 25.92 \text{ V/A} \\ T_i &= \frac{L_{f1}+L_{f2}}{R_{f1}+R_{f2}} = \frac{0.01296}{0.1545} = 0.084 \text{ s} \end{aligned} \tag{26}$$

The parameter τ_i in (26) was set to 0.5 ms in order to ensure the fast response of i_d and i_q without the overshoot. The bandwidth of the current control loops with the utilized controller parameters from (26) amounts to 337 Hz, which is significantly lower than f_{res} = 1200 Hz. In this way, the approximation of the LCL filter with the L filter is justified.

The parameters of the battery current controller were determined based on the battery current control loop shown in Figure 3, by considering the corresponding Bode plot shown in Figure 13. The gain of the battery current open loop ($G_{o\text{-}ibat}$) was compensated by the corresponding PI controller ($G_{PI\text{-}ibat}$) in order to achieve the fast response of the battery current and stable operation of the system. The controller parameters of K_b = 0.446, T_b = 0.04 s were selected to ensure the amplitude margin (*AM*) of the open-loop characteristic ($G_{o\text{-}ibat\text{-}PI}$) not lower than 10 dB. This resulted in the high phase margin (*PM*) of 132°.

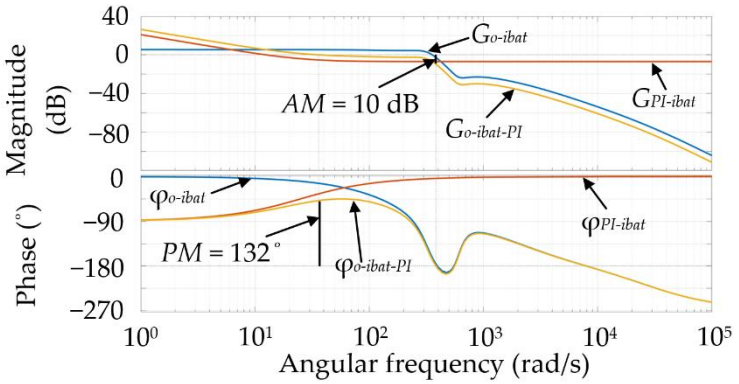


Figure 13. Bode plot of the battery control loop.

Figure 14 shows the Bode plot of the *d*-axis voltage control loop shown in Figure 4. The gain of the open loop without implemented PI controller ($G_{o\text{-}vod}$) was compensated by the PI controller gain ($G_{PI\text{-}vod}$) in order to ensure high crossover frequency and satisfactory phase margin of the resulting open-loop characteristic ($G_{o\text{-}vod\text{-}PI}$). The phase margin of 69° at the crossover frequency of 1000 rad/s was achieved by utilizing the controller parameters K_u = 0.00186 A/V, $T_u = 9.99 \cdot 10^{-5}$ s. This analysis was carried out with the pure resistive, star-connected load of R_t = 53 Ω, resulting in approximately the nominal output power of 3 kW. Note that for the resistive–inductive load, the phase margin becomes even higher, whereas for higher R_t values (i.e., for power lower than nominal), the phase margin slightly decreases.

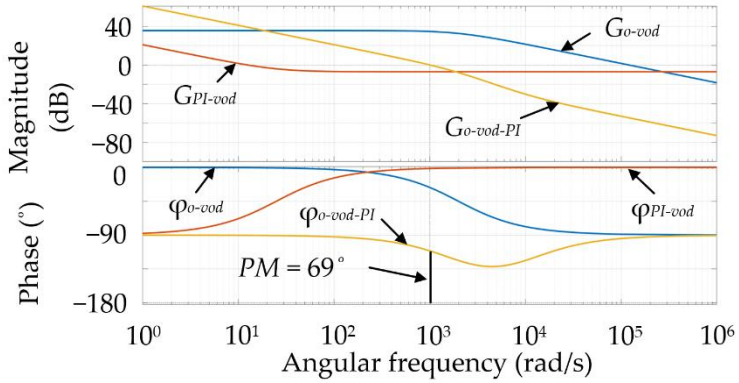


Figure 14. Bode plot of the *d*-axis voltage control loop.

Figure 15 shows the Bode plot of the PV source voltage control loop shown in Figure 5. The corresponding PI controller ($G_{PI\text{-}vpv}$) was utilized to compensate the gain of the PV source voltage open loop ($G_{o\text{-}vpv}$) and to ensure fast response, with overshoots not higher than 10% in order to maintain stable operation of the system. The controller parameters $K_{pv} = 1.88 \cdot 10^{-4}$ V^{-1} and T_{pv} = 0.0166 s ensure the phase margin of 52° of the compensated open-loop characteristics ($G_{o\text{-}vpv\text{-}PI}$), which is considered satisfactory.

As for the MPPT algorithm, the corresponding fixed variation step of v^*_{pv} (Δv_{pv}) was set to 5 V. For this value of Δv_{pv}, the longest transient, of approximately 0.15 s, is noted for the transfer function from d_0 to i_{bat}. Finally, T_{mppt} is set to 0.2 s in order to ensure the proper multitask operation of MicroLabBox, as explained above.

The parameters given above were implemented into the system, which was tested both during the grid-tied operation and the stand-alone operation. The results are presented in the next section.

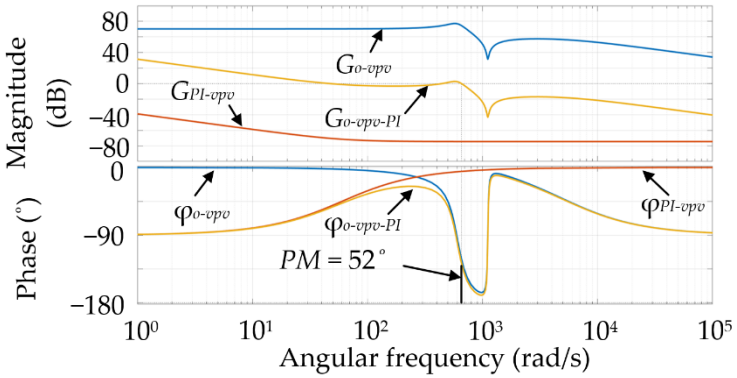


Figure 15. Bode plot of the PV source voltage control loop.

6. Experimental Results

The experimental testing of the considered system was carried out for different operation conditions. During the experimental testing, the irradiance value was varied from 300 W/m^2 to 1000 W/m^2, whereas the PV source temperature was varied from 10 °C to 50 °C. First, the steady-state analysis was carried out to determine the basic features of the considered system, including the accuracy of the proposed MPPT algorithm, the system power distribution, and the efficiency, as well as to gain a more complete insight into the operation of the system. The dynamic analysis of the system, on the other hand, is crucial for the validation of the proposed concept, so it was carried out in a more meticulous way in order to determine the system response with respect to the variation of different system variables, such as the irradiance or the load-resistance value. Note that the value of the PV source power is not required by the proposed control algorithm. Therefore, the PV source power calculation is enabled only in order to determine the static tracking efficiency of the proposed MPPT algorithm. The PV source current has been measured for this purpose by means of the Hall-effect transducers LA 55-P/SP52 (LEM).

6.1. Steady-State Analysis

The steady-state results are shown in Figure 16. The measurements were carried out during the grid-tied operation for the temperatures T_{pv} = 10 °C and T_{pv} = 50 °C, and for all the considered irradiances. The reference battery current was varied in order to achieve different battery power values and, hence, different values of the grid power and current. The increase in the positive (discharging) battery power (p_{bat}) results in an increase in the *d*-axis current injected to the grid (i_d) for approximately the value of $\Delta p_{bat}/(1.5V_{g,max})$, whereas the increase in the negative (charging) battery power results in the decrease in i_d for approximately the value of $\Delta p_{bat}/(1.5V_{g,max})$. Note that the inverter losses remain practically constant during the variation of p_{bat}. As expected, the achieved PV source power (p_{pv}), denoted "x" in Figure 16a, is higher for T_{pv} = 10 °C than for T_{pv} = 50 °C. This power is practically equal to the maximum available PV power ($p_{pv\text{-}MPP}$), denoted "o" in Figure 16a, for all the considered operating points. The static tracking efficiency (*STE*) of the proposed P&O algorithm calculated as $P_{pv}/P_{pv\text{-}MPP}$ for all the considered measurement points is shown in Table 3. The considered efficiency ranges from 96.9% to 100%, which corresponds to the values given in [30,31] for the conventional P&O algorithm. In [31], the efficiency of the conventional algorithm has been approximately 2% lower in the case of irradiance values lower than 600 W/m^2 than in the case of irradiance values higher than 600 W/m^2. Finally, it may be concluded that, by omitting the PV current sensor as in the P&O algorithm proposed in this study, the static tracking efficiency of the algorithm is not adversely affected.

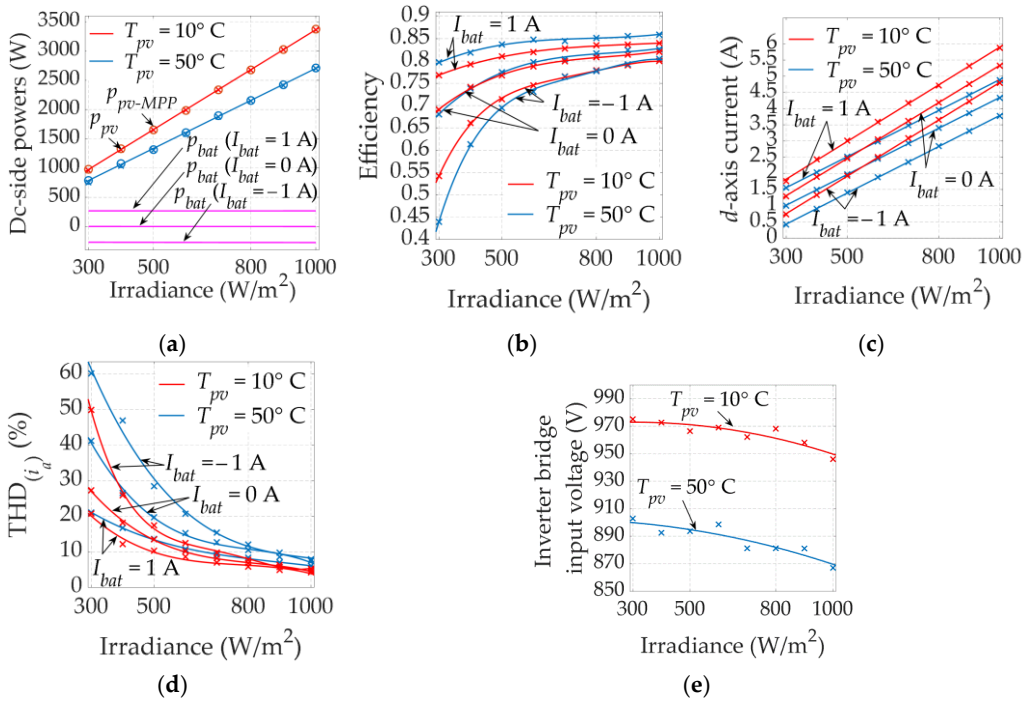


Figure 16. Steady-state characteristics of the considered system: dc-side powers (**a**), efficiency (**b**), *d*-axis current (**c**), THD of phase current (**d**), and input voltage of inverter bridge (**e**).

Table 3. The static tracking efficiency of the proposed P&O algorithm.

Z (W/m^2)	300	400	500	600	700	800	900	1000
$STE_{50°C}$ (%)	96.9	97.2	99.23	98.44	98.94	99.53	99.5	99.63
$STE_{10°C}$ (%)	98.81	98.92	99.87	100	100	99.81	99.9	99.72

In the battery discharging mode (I_{bat} = 1 A), the system efficiency (Figure 16b), calculated as $p_{grid}/(p_{bat} + p_{pv})$, is higher for the higher T_{pv} value in the whole considered range of irradiance values. This increase in efficiency is probably a consequence of lower switching losses of the IGBTs in the inverter bridge in the case of T_{pv} = 50 °C due to the lower input voltage, as shown in Figure 16e. However, as the battery current drops from 1 A to −1 A, the current injected to the grid also drops (Figure 16c), whereas the corresponding THD value rapidly increases (Figure 16d). This implies higher current ripple and, thus, higher value of the high-order harmonics, resulting in higher power losses of the output LCL filter. At some point, an increase in these losses with T_{pv} becomes more dominant than a decrease in switching losses, so the system efficiency starts to drop with T_{pv} (Figure 16b, I_{bat} = −1 A).

6.2. Dynamic Analysis

The dynamic analysis of the considered system was carried out for T_{pv} value of 30 °C during the grid-tied operation and the stand-alone operation. For this type of analysis, the temperature was set to a constant value (in the middle of the considered range) due to the fact that, in real applications, the temperature cannot change abruptly as opposed to the irradiance or load.

6.2.1. Grid-Tied Operation

Figure 17 shows the waveforms of the system variables in the case of the irradiance variation, with the reference battery current set to zero (i^*_{bat} = 0 A). At the beginning, the irradiance (Z) is equal to 600 W/m^2 and changes approximately every 10 s in the following order: 300 W/m^2, 700 W/m^2, 1000 W/m^2, 800 W/m^2. Figure 17a shows that the decrease

in the irradiance causes a decrease in the PV source power. Due to i^*_{bat} = 0 A, the battery power is equal to zero, whereas the variation of the grid power follows the variation of the PV source power. The *d*-axis grid current (i_d) follows the reference value (i^*_d), which varies with the irradiance in order to maintain i^*_{bat} = 0 A, as shown in Figure 17b. On the other hand, the *q*-axis grid current is equal to zero, which ensures the unity power factor. Figure 17c shows that the qZSI input current (i_{L1}) follows the irradiance change, whereas the battery current (i_{bat}) stays equal to the reference value of 0 A. The PV source voltage (v_{pv}) follows v^*_{pv}, generated by the MPPT algorithm, which decreases with the irradiance, as shown in Figure 17d. Finally, Figure 17e shows the duty cycle (d_0) and modulation index (m_a), which are practically constant during the experiment due to the fact the v_{pv} variations were marginal.

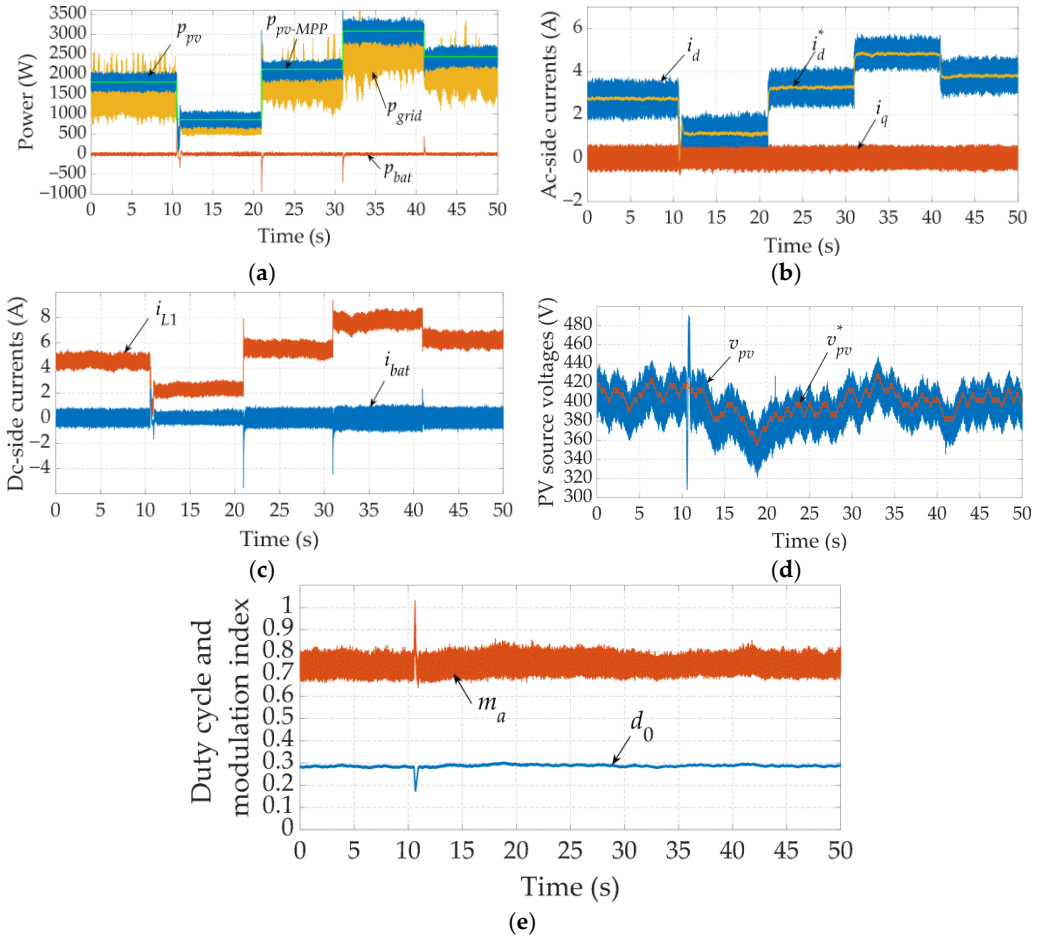


Figure 17. Irradiance variation during the grid-tied operation: system powers (**a**), output grid currents (**b**), dc-side currents (**c**), PV source voltage (**d**), and modulation index and duty cycle (**e**).

It may be seen that the proposed MPPT algorithm accurately tracks the maximum available PV power ($p_{pv\text{-}MPP}$) for all the considered irradiance values, with the fast responses to irradiance variations. On the other hand, the battery controller ensures high robustness to disturbances in the system and zero steady-state error. Note that d_0 and m_a are practically constant during the whole experiment, with the only exception being the transient at t = 11 s, where *Z* decreases in a step manner from 600 W/m^2 to 300 W/m^2. This means that the assumptions utilized for determination of transfer function from i_d to i_{bat}, defined in (17), are justified.

Figure 18 shows the waveforms of the system variables in the case of the reference battery current variation, with *Z* set to 700 W/m^2. At the beginning, i^*_{bat} is set to 0 A and then changes approximately every 10 s in the following order: 1.5 A, 1 A, 2 A, 0 A, −1.5 A,

−1 A, −2 A, 0 A. Figure 18a shows that p_{grid} increases with the p_{bat}, whereas p_{pv} is constant and equal to $p_{pv\text{-}MPP}$ due to the constant values of Z and T_{pv}. The battery current follows its reference value and there is no overshoot in the i_{bat} response during the step variations of i^*_{bat}, as shown in Figure 18c (similar i_{bat} waveforms may be obtained by the utilization of a simulation model of the battery control loop shown in Figure 3). Figure 18d shows that the PV voltage oscillates around the MPP, which is a feature of all P&O algorithms, but with no adverse impact on the system performance. The modulation index and the duty cycle are practically unaffected by i^*_{bat} variations, as shown in Figure 18e.

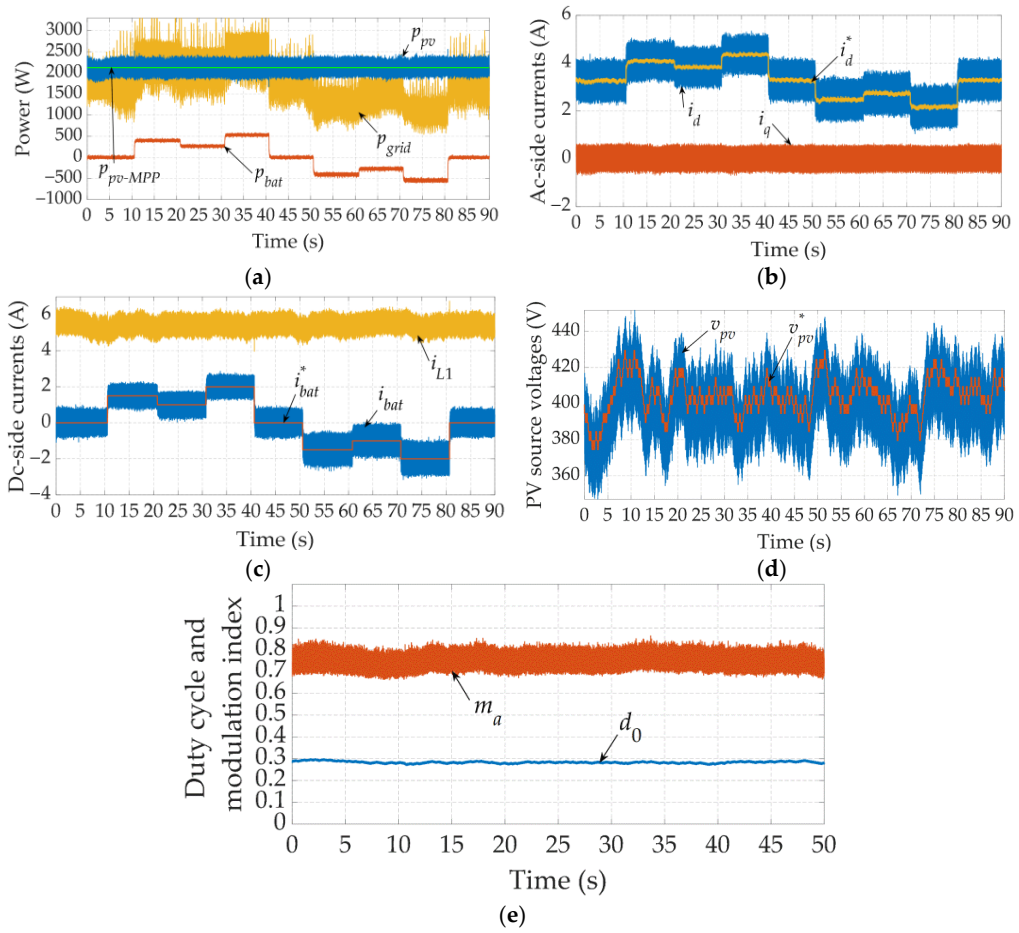


Figure 18. Reference battery current variation during the grid-tied operation: system powers (**a**), output grid currents (**b**), dc-side currents (**c**), PV source voltage (**d**), and modulation index and duty cycle (**e**).

6.2.2. Stand-Alone Operation

Figure 19 shows the responses recorded for the case of the irradiance and load resistance variation with $V_{l,max}$ set to 340 V in order to ensure approximately the same output voltage level as in the utility grid. At the beginning, Z is equal to 600 W/m^2 and it is varied at 12 s, 22 s, 41 s, and 51 s, in the following order: 300 W/m^2, 700 W/m^2, 1000 W/m^2, 800 W/m^2, respectively. On the other hand, the load resistance is changed at 32 s from 175 Ω to 90 Ω (i.e., the load power is increased from 990 W to 1926 W). Figure 19a shows that p_{pv} follows $p_{pv\text{-}MPP}$ as accurately as during the grid-tied operation and is not affected by the load resistance variation. i_d increases with the load power with a smooth transient, whereas i_q is equal to zero due to the applied pure resistive load, as shown in Figure 19b. The battery current in this operation is not controlled, so it increases with the irradiance decrease. As a result of the decrease in the load resistance, i_{bat} increases to cover the load power requirements.

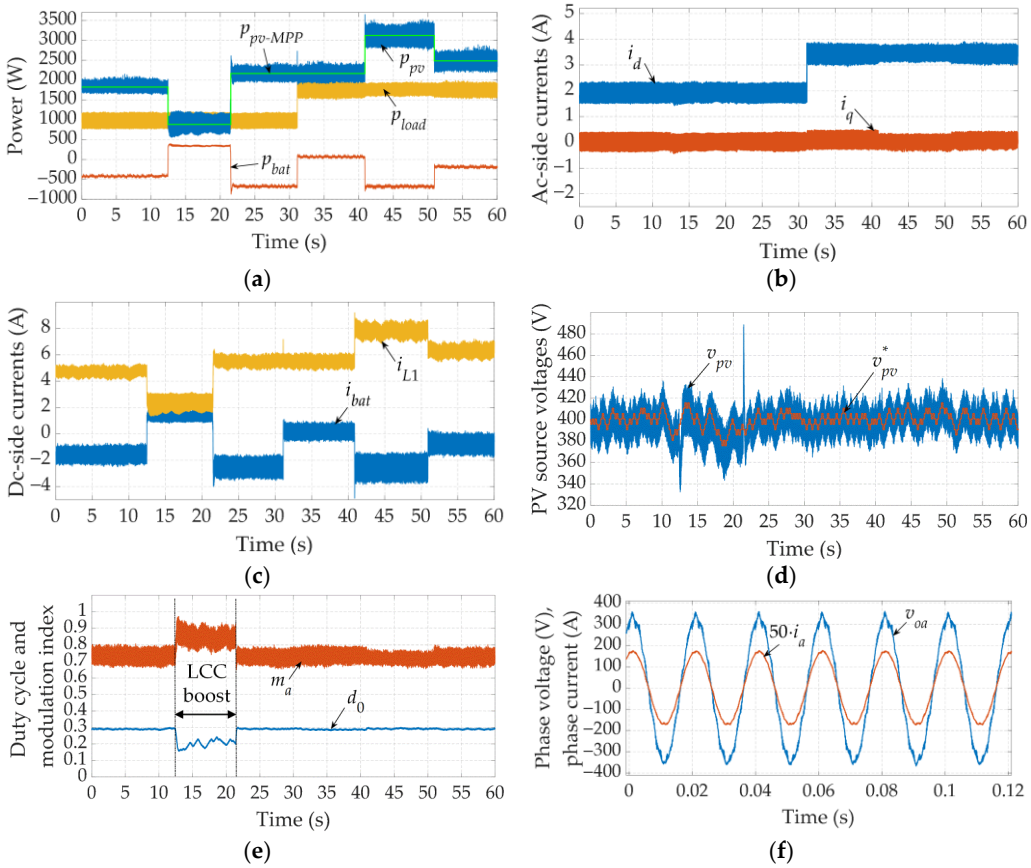


Figure 19. Irradiance variation and load resistance variation during the stand-alone operation: system powers (**a**), output load currents (**b**), dc-side currents (**c**), PV source voltage (**d**), modulation index and duty cycle (**e**), and phase voltage and current (**f**).

Note in Figure 19e that, in the case of Z = 300 W/m^2, the values of the modulation index and duty cycle are significantly different than in the case of higher irradiances. This is due to the occurrence of the so-called load-caused current (LCC) boost [32–34], where the impedance network diode blocks during the non-ST state, which is normally not the case. However, this does not affect the MPPT algorithm, which still achieves tracking of $p_{pv\text{-}MPP}$. In this study, the LCC boost has been detected online as described in Appendix B. Note that all the variables required for the LCC boost detection are already known in the considered control algorithm. Figure 19f shows the phase voltage (v_{oa}) and current (i_a), which are in this case practically sinusoidal (THD ≈ 4%).

The same experiment as in Figure 19 was performed for the case of the non-linear load, which was composed of the three-phase full-bridge diode rectifier and the resistive load. Figure 20 shows that the system performance was equally as good as in the case of the linear resistive load. Figure 20f shows that v_{oa} is slightly more distorted (THD ≈ 7%) despite of the existence of the low-order harmonics in i_a. It is assumed that the distortion of the phase currents causes the ripple of i_d and i_q to be higher than in case of the linear load.

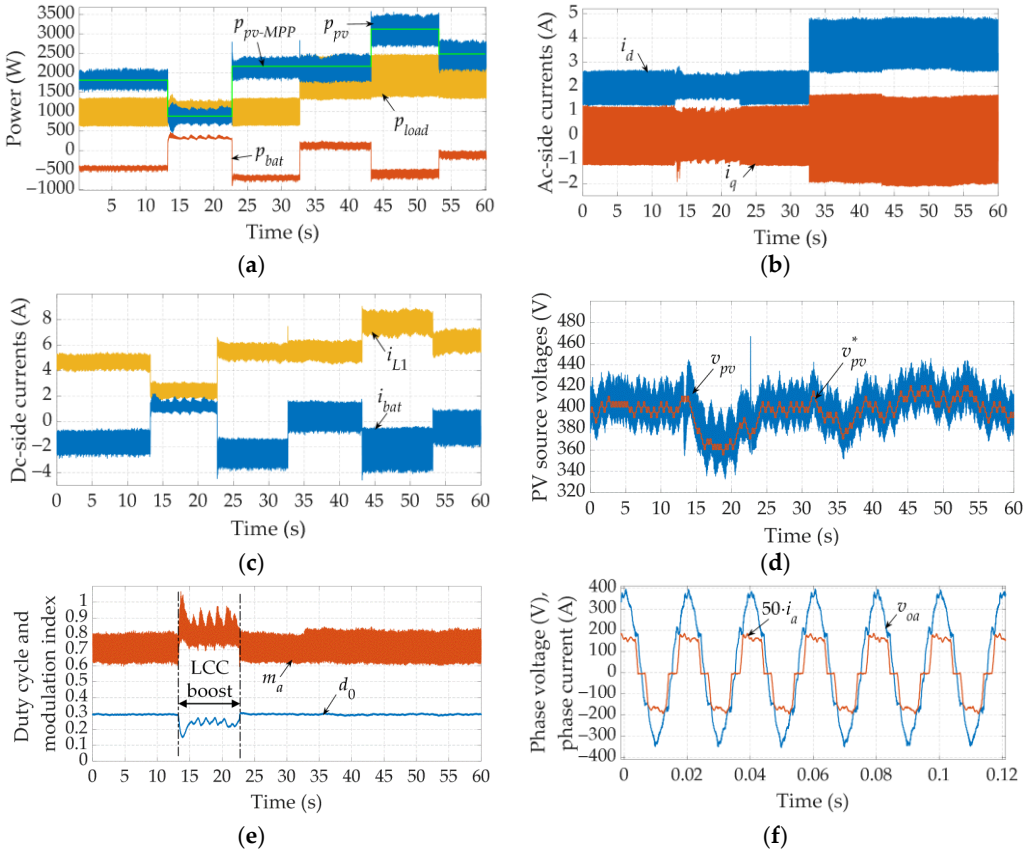


Figure 20. Irradiance variation and non-linear load resistance variation during the stand-alone operation: system powers (**a**), output load currents (**b**), dc-side currents (**c**), PV source voltage (**d**), modulation index and duty cycle (**e**), and phase voltage and current (**f**).

Figure 21 shows the waveforms recorded for the case of $MBC = 0$ and $MBC = 1$ for different irradiance values and the load resistance value of 175 Ω. At the beginning, $MBC = 0$, $Z = 700$ W/m^2, and $p_{pv} = p_{pv\text{-}MPP}$, resulting in battery charging of approximately 600 W. At $t = 11$ s, the batteries are fully charged, MBC changes to 1 and p_{pv} departs from $p_{pv\text{-}MPP}$ by increasing v^*_{pv} to achieve $i_{bat} \approx 0$ A and prevent further charging of the batteries. The length of the respective transient period is approximately 1.5 s. Further, at $t = 26$ s, the irradiance decreases to 600 W/m^2, resulting in a transient period of approximately 2 s. After this transient, the batteries were slightly discharging because of the error related to the Δv^*_{pv} value, as described above. At $t = 41$ s, the irradiance decreases to 300 W/m^2 and the battery current becomes positive (discharging) due to the low PV source power. Consequently, p_{pv} is again set equal to $p_{pv\text{-}MPP}$ by the control algorithm to achieve minimum discharging current. At $t = 56$ s, the irradiance increases to 500 W/m^2, causing a rapid increase in the PV source power, which results in negative i_{bat} (charging). As a result, the control algorithm increases v^*_{pv} to achieve $i_{bat} \approx 0$ A, which is accomplished in approximately 2.5 s. Finally, at $t = 71$ s, MBC becomes 0, allowing the batteries to be charged again. Consequently, v^*_{pv} decreases to ensure $p_{pv} = p_{pv\text{-}MPP}$, which is accomplished in approximately 1.5 s.

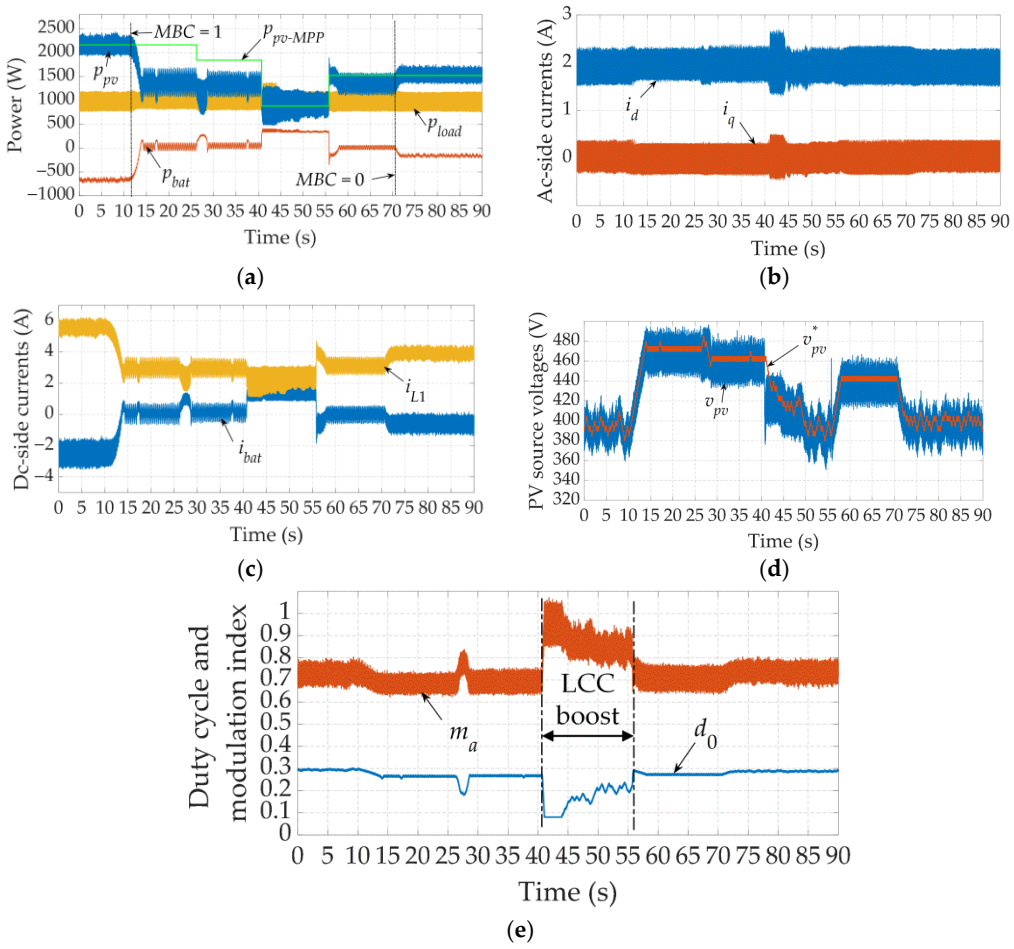


Figure 21. Irradiance variation and maximum battery charge signal variation during the stand-alone operation: system powers (**a**), output load currents (**b**), dc-side currents (**c**), PV source voltage (**d**), and modulation index and duty cycle (**e**).

7. Conclusions

The accuracy of the three derived transfer functions utilized for the control system design was found to be satisfactory, with the maximum steady-state errors of the calculated responses not surpassing 12%. The dynamic transients obtained by the transfer functions from the *d*-axis current to the battery current and from the duty cycle to the PV source voltage corresponded to measurements with negligible error. This confirmed the accuracy of the proposed small-signal model and allowed these two transfer functions to be utilized for PI controller tuning and the analysis of the system stability. In addition, the settling times of the transients obtained by the transfer function from the duty cycle to the battery current matched well with those obtained experimentally. This allowed the considered transfer function to be utilized for the determination of the tracking period of the MPPT algorithm because the longest settling time of the battery current response is noted for step changes in the duty cycle.

The recorded experimental responses of the system variables to the rapid changes in the irradiance and the reference battery current during the grid-tied operation confirm excellent MPP tracking and stable operation. A maximum settling time of 0.4 s is noted for the abrupt decrease in the PV source power of 1000 W, whereas the static tracking efficiency of the proposed MPPT algorithm ranged from 96.9% to 100%. As for the reference battery current variations, the settling time of all the considered transients amounted to approximately 0.3 s. During the stand-alone operation, the MPP tracking was again excellent and the system responded to the rapid changes in the irradiance as well as during the grid-tied operation. This confirms the validity of the proposed MPPT algorithm, whose

utilization reduces system implementation costs due to the elimination of one current sensor compared to the conventional P&O algorithm. During the rapid changes in the load power (both for the linear and the non-linear load), the settling time amounted to approximately 0.2 s. Finally, it was shown that the implementation of the maximum battery charge signal during the stand-alone operation prevents overcharging of the batteries by setting the battery current approximately to zero.

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Appendix A

Three inductors, all with inductances of 4.32 mH, were available. Two inductors were placed on the inverter side (L_{f1} = 8.64 mH), whereas one was placed on the grid side (L_{f2} = 4.32 mH). The capacitance C_f was obtained as follows [35]:

$$C_f = \frac{7}{100}\frac{I_n}{20\omega V_n} = \frac{7}{100}\frac{P_n}{3\omega V_n^2} = \frac{7}{100}\frac{3000}{3 \cdot 314.159 \cdot 230^2} \approx 4\ \mu\text{F} \quad \text{(A1)}$$

In (A1), I_n and V_n represent RMS phase current and voltage, respectively. Selected C_f ensures the reactive power of filter capacitors not to be higher than 7% of nominal power (P_n) (recommendation 5–10%). In this way, the resonant frequency (f_{res}) of 1200 Hz, calculated in (25), meets the following condition [36]:

$$10f < f_{res} < f_{sw}/2 \quad \text{(A2)}$$

where f represents the fundamental frequency of the output inverter voltage/current (50 Hz in this study), whereas f_{sw} represents the switching frequency (5 kHz in this study).

Finally, the corresponding damping resistance is obtained as follows [37]:

$$R_d = \frac{1}{3}\frac{1}{2\pi f_{res} C_f} \approx 10\Omega \quad \text{(A3)}$$

Appendix B

The load-caused current (LCC) boost is characterized by the diode in the qZSI impedance network blocking during the non-ST state. Based on the equivalent circuit for the non-ST state, shown in Figure 2a, the LCC boost occurs if the following condition is met:

$$i_{pn} > i_{L1} + i_{L2} \quad \text{(A4)}$$

The occurrence of the LCC boost causes the unintended boost increase. The existence of the PV source voltage controller in this study eliminates the potential adverse effects of the LCC boost.

In the case of the ideal qZSI, with considered sinusoidal output currents, the maximum value of i_{pn} is equal to the peak phase current $I_{ph,max}$. Figure A1 shows the current of both the impedance network inductors. The LCC boost certainly will not occur if:

$$I_{L1,min} + I_{L2,min} > I_{ph,max} \tag{A5}$$

The minimum values of the inductor currents $I_{L1,min}$, $I_{L2,min}$ are calculated as:

$$\begin{aligned} I_{L1,min} &= I_{L1} - \frac{\Delta I_{L1}}{2} \\ I_{L2,min} &= I_{L2} - \frac{\Delta I_{L2}}{2} \end{aligned} \tag{A6}$$

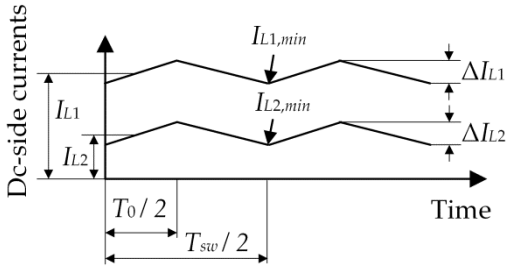

Figure A1. Waveforms of the dc-side currents.

The current ripples in (A6) are considered equal and may be calculated according to the equivalent circuit for the ST state, shown in Figure 2b, as follows:

$$\Delta I_{L1} = \Delta I_{L2} = \frac{V_{C1} T_0}{2L} \tag{A7}$$

By applying (A6) and (A7), (A5) becomes:

$$I_{L1} + I_{L2} - \frac{V_{C1} T_0}{2L} > I_{ph,max} \tag{A8}$$

By applying $I_{L2} = I_{L1} - I_{bat}$ and $I_{L1} = P_{pv}/V_{pv}$, (A5) becomes:

$$2\frac{P_{pv}}{V_{pv}} - I_{bat} - \frac{V_{C1} T_0}{2L} > I_{ph,max} \tag{A9}$$

In the case of the ideal qZSI, the following applies:

$$\begin{aligned} &P_{pv} + P_{bat} = P_{out} \\ &P_{bat} = I_{bat} V_{bat} \\ &P_{out} = 3\frac{V_{ph,max}}{2} I_{ph,max} \cos\phi = \frac{3}{4} V_{pv} M_a \frac{I_{ph,max} \cos\phi}{1-2d_0} = \frac{3}{8Z_l} \cos\phi \frac{V_{pv}^2 M_a^2}{(1-2d_0)^2} \\ &V_{C1} = \frac{1-d_0}{1-2d_0} V_{pv}; V_{bat} = \frac{d_0}{1-2d_0} V_{pv} \end{aligned} \tag{A10}$$

In (A10), capital letters represent the mean values of the considered variables. $V_{ph,max}$ represents the peak phase voltage, whereas Z_l represents the equivalent output impedance, which may be obtained as $V_{ph,max}/I_{ph,max}$. Finally, by applying (A10), (A9) becomes:

$$\frac{3\cos\phi M_a^2}{4Z_l(1-2d_0)} - \frac{T_0(1-d_0)}{2L} - \frac{I_{bat}}{V_{pv}} > \frac{M_a^2}{2Z_l} \tag{A11}$$

Equation (A11) has been utilized for the online detection of the LCC boost during the experimental investigation of the considered system.

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ŽIVOTOPIS

Rođen sam 17. listopada 1993. godine u Mostaru gdje sam završio osnovnu školu i Srednju elektrotehničku školu Ruđera Boškovića 2012. godine.

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Državljanin sam Republike Hrvatske i Bosne i Hercegovine te oženjen suprugom Irenom.

BIOGRAPHY

I was born on October 17, 1993 in Mostar where I graduated from elementary school and Ruđer Bošković High School of Electrical Engineering in 2012.

In 2012, I enrolled in the undergraduate study program of Electrical Engineering and Information Technology at the University of Split, Faculty of Electrical Engineering, Mechanical Engineering and Naval Architecture. I finished this study program in 2015, and in the same year I enrolled in the graduate study program of Electrical Engineering, majoring in Automation and Drives, at the same faculty. I finished this study in 2017 and earned the title of Master of Electrical Engineering.

Since October 1, 2017, I have been employed at the University of Split, Faculty of Electrical Engineering, Mechanical Engineering and Naval Architecture as an assistant at the Department of Power Engineering. I have been involved in teaching activities involving auditory and laboratory exercises from the following courses: Control Engineering, Digital Electronic, and Digital Engineering. I enrolled in the PhD study in Electrical Engineering and Information Technology at the Faculty of Electrical Engineering, Mechanical Engineering and Naval Architecture in October 2017. During this study program, I participated as a researcher in the Croatian Science Foundation's project titled Wind-Solar System for Optimized Residential Electric Generation.

During my PhD studies, I have prepared and published ten scientific papers as the first author. Four of them were published in journals indexed in the WoSCC database, one of them was published in a journal indexed in the SCOPUS database, whereas the remaining five were published in the proceedings of international scientific conferences. In addition, I have co-authored fifteen other scientific papers.

I am a citizen of the Republic of Croatia and Bosnia and Herzegovina and married to my wife Irena.